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Design of S-Band Frequency Synthesizer for Microwave Applications

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ABSTRACT: A phase locked loop based indirect frequency synthesizer is designed for S-band frequency. A Phase locked loop is designed and the phase noise response and transient response of the designed PLL is simulated for 2100MHz frequency. The phase noise response of total PLL and its individual components are obtained. A 3rd order low pass passive loop filter is used and by varying the loop bandwidth and phase margin the trade-off between lock time and phase noise is observed and an optimum value of loop bandwidth and phase margin is chosen such that its phase noise contribution is less. The designed phase locked loop has a low phase noise value of -112.4dBc/Hz at 100 kHz offset frequency and has a fast lock time of 119.5 us. The time taken by the designed frequency synthesizer to lock to 10 Hz frequency error and 1° phase error under transient conditions is found to be 149 us and 116 us respectively. The RMS phase jitter obtained for the designed phase locked loop is 0.3° rms. The phase locked loop is designed and simulated using ADIsimPLL tool. The phase locked loop design aims at achieving low phase noise, reduced lock time and high reliability for S-band applications.

KEYWORDS: Phase locked loop, integer-N PLL, loop filter, phase noise, lock time.

1 INTRODUCTION

Frequency synthesizers are key component in any communication systems from satellite receivers to mobile phones. PLL based indirect frequency synthesizers are used as local oscillators for producing stable high frequency output in wireless communication systems. Direct frequency synthesizers have high speed, low noise but because of their complex size and high power consumption in this paper we use indirect synthesis technique. The indirect synthesis technique which generates the output frequency by utilizing a feedback system is less complex and produces low phase noise and low spurs.

In this paper, an S-band PLL frequency synthesizer at 2.1 GHz is designed. To predict the phase noise contributions a phase locked loop is designed and simulated. The design is simulated for different loop bandwidth and phase margin. The resultant phase noise and lock time are analyzed and an optimum value of loop bandwidth and phase margin is chosen to obtain better phase noise performance and fast locking.

A PLL is a circuit that causes a particular system to track with another one. More precisely, a PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in frequency as well as in phase. In the synchronized—often called "locked"—state, the phase error between the oscillator's output signal and the reference signal is zero, or it remains constant [4]. The basic block diagram of a PLL system is given in Fig. 1

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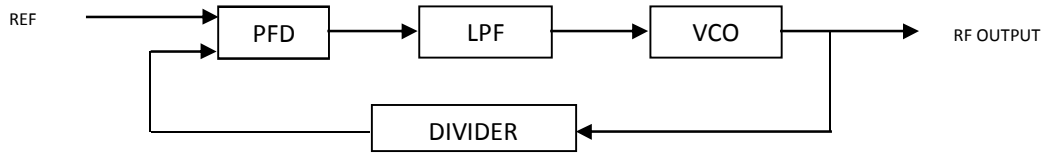

Fig. 1. PLL Block Diagram

The frequency synthesizer is designed using ANALOG DEVICES- ADF4351 integrated synthesizer with VCO. The ADF4351 allows implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and external reference frequency. The ADF4351has an integrated voltage controlled oscillator (VCO) with a fundamental output frequency ranging from 2200MHz to 4400MHz. The device operates with a power supply ranging from 3.0 V to 3.6 V. Control of all on-chip registers is through a simple 3-wire interface [5].

The RF VCO frequency (RFOUT) equation is [5]

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

Where, RF_{OUT} is the output frequency of the voltage controlled oscillator (VCO), INT is the preset divide ratio of the binary 16-bit counter (23 to 65,535 for the 4/5 prescaler; 75 to 65,535 for the 8/9 prescaler), FRAC is the numerator of the fractional division (0 to MOD − 1), MOD is the preset fractional modulus (2 to 4095).

2 3RD ORDER LOOP FILTER DESIGN AND OPTIMIZATION

Passive loop filters are used widely in the frequency synthesizers for converting the current pulses output of charge pump into error voltage for tuning the voltage controlled oscillator. A 3rd order loop filter is used for designing the frequency synthesizer. The topology of the 3rd order loop filter used in the design of the PLL is given in Fig. 2

Having low phase noise in communication systems will improve the data transmission and having a fast lock time will decrease the power consumption. Hence the system should have an optimum phase noise performance and fast lock time.

The capacitor C1 is added, because it reduces the spurs level significantly. Also the components R3 and C3 can optionally be added in order to further the reference spur level [2].

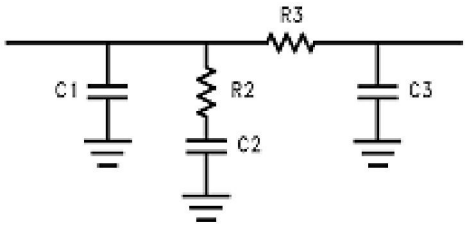

Fig. 2. Passive low pass loop filter

2.1 LOOP BANDWIDTH OPTIMIZATION

Using Narrow loop bandwidths will remove unwanted spurious signals from the synthesizer output, but it also increases the lock time. Using a wider loop bandwidth reduces lock times but leads to increased spurious signals inside the loop bandwidth. The PLL design is simulated for various loop bandwidths and the obtained phase noise and lock time are analyzed.

Table 1. Simulated Phase Noise and Lock Time for various Loop Bandwidth

Loop Bandwidth(kHz)	Phase noise(dBc/Hz)	Lock time(us)
10	-116.0	672
15	-115.5	370
20	-114.8	245
25	-113.7	186
30	-112.4	149
35	-111.1	130
40	-109.8	113
45	-108.5	109
50	-107.3	99.7
55	-106.3	92.5
60	-105.4	86.5
65	-104.6	81.4

From the values in table 1 it can be seen that as the loop bandwidth increases the lock time decreases but phase noise increases. Hence an optimum value of 30 kHz loop bandwidth is chosen.

2.2 PHASE MARGIN OPTIMIZATION

The phase margin denotes how far the PLL system is from instability. Typical value of phase margin ranges from 40^0 to 70^0. Increasing the phase margin increases the phase noise and reduces the lock time.

Table 2. Simulated Phase Noise and Lock Time for various Phase Margin

Loop Bandwidth(kHz)	Phase noise(dBc/Hz)	Lock time(us)
35	-113.2	199
40	-112.8	167
45	-112.4	149
50	-112.0	190

From the table 2 it can be seen that increasing the phase margin reduces the lock time. But after 45^0 phase margin the lock time increases. Hence an optimum value of 45^0 phase margin is chosen.

The following parameters are used for designing the loop filter:

- I_{CP}= 5.0 mA
- K_V = 40 MHz/V
- F_{PFD} = 10 MHz
- Loop bandwidth: 30 kHz
- Phase margin: 45^0

3 PLL DESIGN AND SIMULATION USING ADISIMPLL

The Phase locked loop is designed using ANALOG DEVICES PLL chip ADF4351 for an operating frequency of 2100 MHz with designed 3rd order loop filter and a reference frequency of 10 MHz using ADIsimPLL software. The schematic of designed PLL is given in the Fig. 3

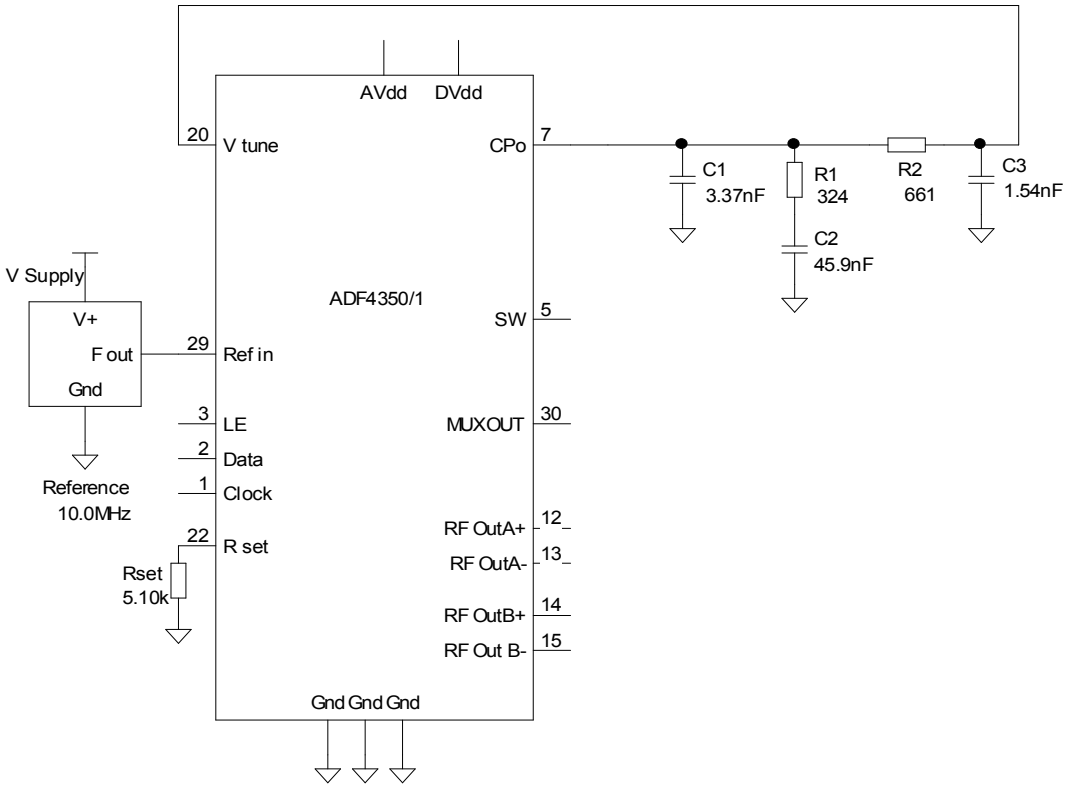

Fig. 3. PLL Schematic using ADIsimPLL

The phase locked loop design is simulated and the simulation results for 2100MHz operating frequency with a comparison frequency of 10 MHz are obtained. Total phase noise of the PLL and also phase noise curves of various individual components like loop filter, VCO and PLL chip are given in the fig. 3.

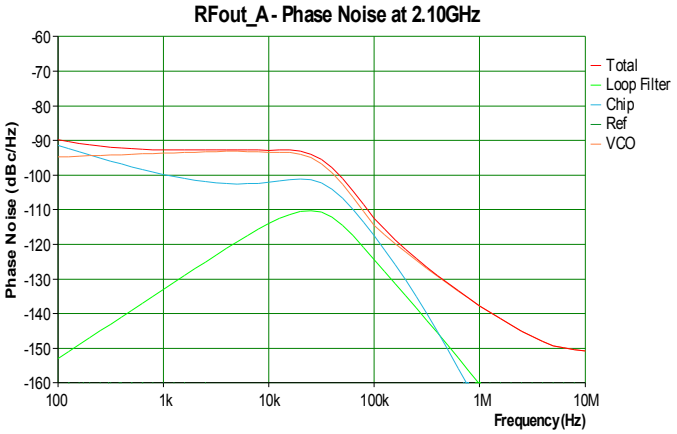

Fig. 4. Phase Noise of Total System and Individual Components

The table 3 shows the total phase noise of the PLL and also phase noise curves of various individual components like loop filter, VCO and PLL chip for various offset frequencies. The phase noise obtained at 100k offset frequency is -112.4dBc/Hz.

Table 3. Phase Noise Results

Frequency Offset(kHz)	Total	VCO	Chip	Filter
100	-89.70	-94.73	-91.34	-153.0
1.00k	-92.69	-93.64	-99.76	-133.0
10.0k	-92.89	-93.49	-102.1	-114.0
100k	-112.4	-114.5	-117.5	-124.3
1.00M	-137.7	-137.7	-167.4	-160.5

The output frequency of the PLL is shown in fig. 4. The time taken by the frequency synthesizer to lock to 2.1GHz frequency is 119.52us. This lock time is optimum for the PLL synthesizer to be used in wireless communication system applications.

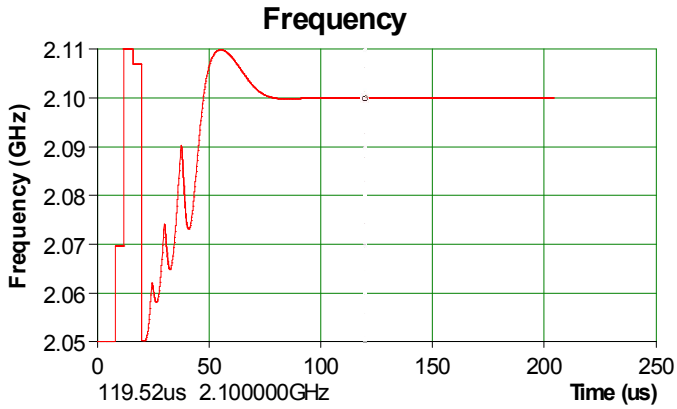

Fig. 5. PLL Output Frequency

The output phase error of the PLL system is given in fig.6. This plot shows the output phase error at the output of PLL during transient conditions. It can be seen that the Time to lock to 1.0 deg phase error is 116us.

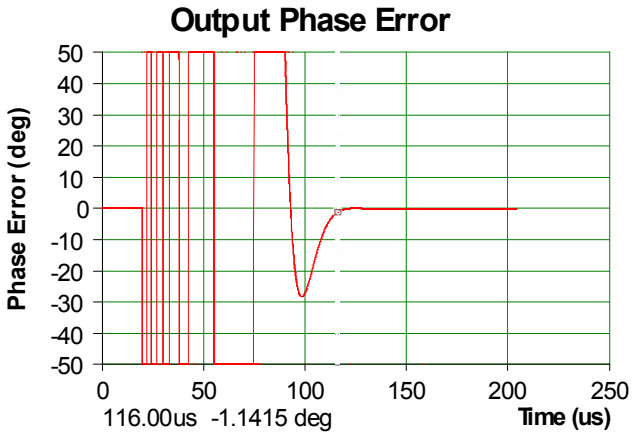

Fig. 6. PLL Output Phase Error

The output frequency error of PLL during transient condition is given in fig.7. The time to lock to 10 Hz frequency error is 149us.

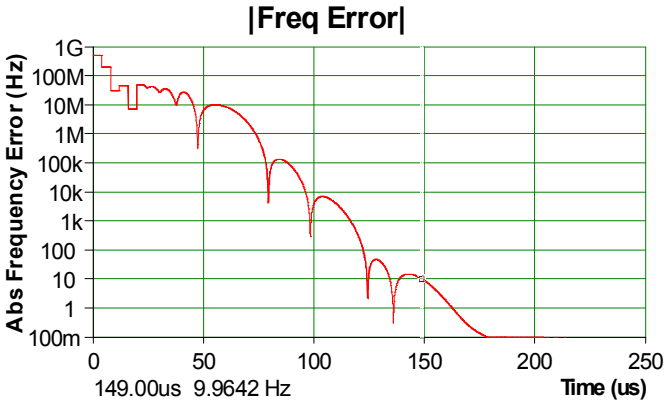

Fig. 7. PLL Output Frequency Error

The system maximum phase error specification for GSM receivers/transmitters (Rx/Tx) is 5° rms [1]. The RMS phase jitter obtained for the simulated phase locked loop is 0.3^0 rms.

4 CONCLUSION

This paper presents a design of S-band frequency synthesizer for microwave application. An optimum value of loop bandwidth and phase margin is obtained by simulating the phase locked loop for various values of loop bandwidth and phase margin and analyzing the resultant lock time and phase noise. A 3^{rd} order passive loop filter with 30 kHz bandwidth and 45^0 phase margin is used in designing the frequency synthesizer. The phase locked loop is designed and simulated by ANALOG DEVICES PLL chip ADF4351. This design has reduced phase noise and lock time for use in wireless communication systems.

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