International Journal of Innovation and Applied Studies
ISSN 2028-9324 Vol. 9 No. 4 Dec. 2014, pp. 1541-1546

http://www.ijias.issr-journals.org/

Design and Implementation of Efficient Elevator Control System using FPGA

Muhammad Ahsan Ullah[1] and M. A. Saeed[2]

[1]Electronic Engineering Department,
Islamia University, Bahawalpur, Pakistan

[2]Faculty of Electrical Engineering,
GIK Institute, Topi, Pakistan

ABSTRACT: Many industrial and control applications are running through conventional PLC technology adequately because PLC provides flexibility, lower cost and security compared to other control techniques, but still a more powerful alternative is needed. In recent years, FPGA's becomes the best replacement of PLC to implement control algorithms in industrial, digital signal processing, video and audio applications and as well to perform control tasks. The basic dilemma of FPGA's is that it requires an expertise in control automation applications. In this paper, an efficient methodology is proposed to implement PLC state diagram on FPGA using Xilinx StateCAD tool. Three level efficient elevator control system is designed which can be used for different elevator control system having different number of floors. Simply changing the state diagram, VERILOG HDL(Hardware Description Language) code is generated and used in XILINX ISE 7.1i to implement control system on FPGA Spartan-3. StateBench simulator is used to simulate results of proposed control system.

KEYWORDS: Programmable Logic Controller; Field Programmable Gate Array; State Diagram, StateCAD; Hardware Description Language

1 INTRODUCTION

An elevator or lift is transport equipment which is located vertically in the building to take luggage or passenger from one floor to another. Mostly elevators are power-driven by electric motors. Elevators plays vital role in both commercial residential locations. The main operational principal of elevators is the conversion of electrical energy into mechanical energy. The early elevators were considered as cabs and driven by hands or by animals or by rope. The creation of screw drive based system was the significant step in elevator's designs, which finally led to the design of latest modern elevators [1]. Traditional elevator control system is based on Relay logic, PLC and Microcontroller etc. but these systems have reduced number of inputs and outputs [2]. FPGA technology is the best replacement of Relay logic, PLC and Microcontroller due to its flexibility, lower cost, efficiency, security, operational speed and parallel processing ([3], [4]). For the implementation of different hardware architectures, the option of reconfiguring the FPGAs by software makes it better option ([5], [6]).PLC's are still preferred in industrial and automation applications but it does not cover all the practical applications. For this reason, researchers are still investigating for other alternatives. One of the best choices for control applications is to implement control algorithms on FPGA. System performance is improved due to parallel processing of PLC instructions. As soon as possible technique to share allocated sources is used to implement different arithmetic operations with single atomic units as used by [3].

A state diagram is simply used to explain the state machine automation graphically. StateCAD is used to implement state diagram of elevator control system, which is a graphical tool that express ideas of state machines, as state diagrams [7]. After making state diagram StateCAD convert the state diagram into Hardware Description Language (HDL) that can be used as source file in Xilinx Project and changed into schematic symbol Xilinx StateCAD include StateBench which is used to see results as waveforms simulation.

Corresponding Author: M. A. Saeed

The elevator control system is basically finite state machine (FSM). FSM is a digital sequential circuit that consists on different defined states that are controlled by inputs. Finite state machines categorized in two types Asynchronous and Synchronous FSMs. Asynchronous FSMs also called Moore machines in which output depends only on the current state while synchronous FSMs also called Mealy machine in which outputs is generated by using current state and the input variables. The given elevator control system is based on Mealy machine [8].

This paper explains the design of elevator control system by using commercially existing design tool StateCAD from which Verilog HDL code is generated. The key point of this research is that there is no need to write a complex code for control system as needed in other control techniques rather that to use simple approach of state machines to implement PLC state diagram on FPGA for elevator control system deliberately.

2 ALGORITHM FOR ELEVATOR CONTROL SYSTEM

- At any floor when input button is pressed to reach any desired floor the state will be changed.
- According to this state the motor move the car upward or downward.
- As car reached at desired floor, limiter or sensor generate an input to change the state.
- At this state output “00” generated to the H-bridge which will stop the car motor.
- According to next instruction (input) the same procedure repeat.

3 DESCRIPTION OF ELEVATOR CONTROL SYSTEM

There are seven states for three level elevator control systems. To control the elevator system on each floor, input request are provided and push buttons are used for these requests, as shown in Fig. 1. Description of elevator control system is specified in Tab. 1.

- Three states F1, F2, F3 represent the floors.
- Two states MU2, MU3 represents the state for which motor rotates in upward direction.
- At MU2, MU3 states output HBRG=”01” is generated which is attached to H-bridge to control the direction of motor.
- Two states MD1, MD2 represent the state for which motor rotates in downward direction.
- At MD1, MD2 states output HBRG=”10” is generated which is attached to H-bridge to control the direction of motor.
- The transitions PB1, PB2, PB3 are inputs connected to Push buttons.
- The transitions S1, S2, S3 are inputs which are connected to sensors.

The inputs of the elevator control system can be changed any time in StateBench simulator to see the simulation for these inputs. A state can be changed in simulator and the simulator will adjust the inputs automatically. The motor derive the car when the input is given through keyboard. The presence of a car is detected through a sensor attached to each floor.

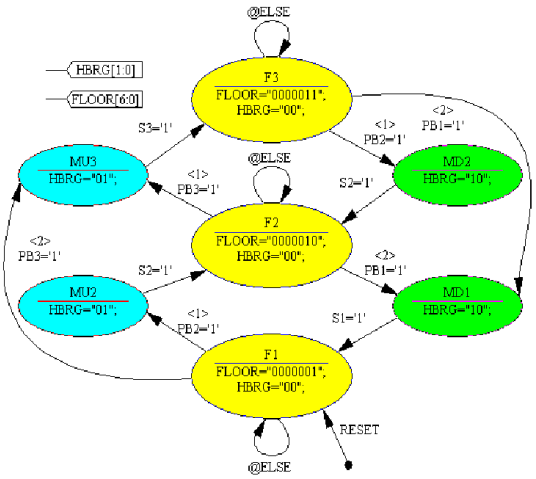

Fig. 1. Elevator control system

Table 1. State and input/ output ports

State Name	Description
Floor States	F1, F2, F3
Moving States (Moving Motor Up-ward) (Moving Motor Down-ward)	MU2, MU3 MD1,MD2
Input Transition (Push Button) (Sensor)	 PB1, PB2, PB3 S1,S2,S3
Outputs	HBRG[0:1] FLOOR[0:6]

4 WORKING MECHANISM

At state F1, when PB1 is pressed, the state remains same using Else transition as shown in Fig 2.

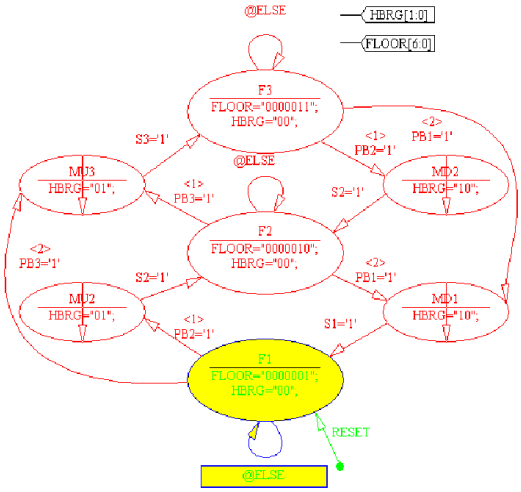

Fig. 2. Diagram for Floor 1

When PB2 is pressed the state changes into MU2 state as shown in Fig. 3 and output HBRG=”01” is generated and motor starts to rotate upward. When sensor S2 is detected due to transition S2 at that state, state will change to F2 state as shown in Fig. 4. Output HBRG=”00” is generated which stops the motor and one instruction is completed. At F1, When PB3 is pressed the state changes into MU3, output HBRG=”01” is generated and motor starts to rotate upward. When sensor S3 is detected due to transition S3 at that state, state will change to F3. Output HBRG=”00” is generated which stops the motor and one instruction is completed. At state F2, F3 the instructions for inputs PB1, PB2, PB3 will executed in the same manner.

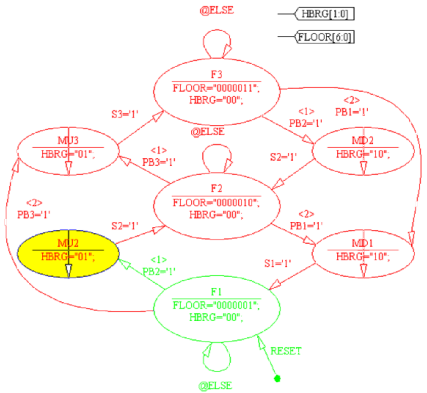

Fig. 3. Diagram for transition between floors

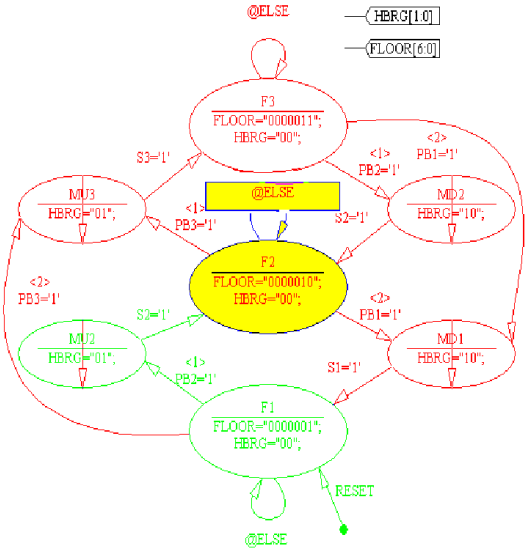

Fig. 4. Diagram for floor 2

5 IMPLEMENTATION

FPGA design work flow of elevator control system is shown in Fig 5. First "logic function " is created as state diagram using Xilinx StateCAD tool, HDL code generated from state diagram which is used in Xilinx Project Navigator to analyze register transfer level (RTL) schematic as shown in Fig 5 Finally, the generated binary file by Xilinx ISE 7.1 is downloaded in FPGA which now behaves according to control algorithm written in StateCAD.

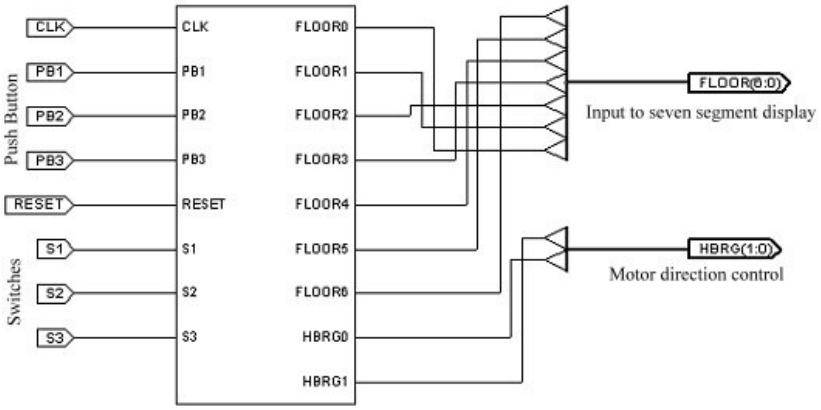

Fig. 5. RTL schematic diagram

As applied system for three floors, PB1, PB2, PB3 represent the input push buttons. S1, S2, S3 represents inputs generated by sensors. Push buttons are used to give instruction for desired floor and sensor used as input to stop elevator car at desired floor. HBRG and FLOOR is output vector, Output H-bridge (HBRG) control the direction of motor rotation, FLOOR output is to shows the floor number accordingly on seven segment display.

According to transition state will be changed, input/output detail is given in Tab. 2. Synthesis results for Spartan-3 implementation are shown in Tab. 3.

Table 2. Ports description

Port Name	Type	Width	Remarks
CLK	Input	1	Clock
PB1	Input	1	Push Button 1
PB2	Input	1	Push Button 2
PB3	Input	1	Push Button 3
RESET	Input	1	RESET
S1	Input	1	Sensor 1
S1	Input	1	Sensor 2
S3	Input	1	Sensor 3
FLOOR	Output	6	Floor number display
HBRG	Output	4	H-Bridge

Table 3. Synthesis results for Spartan-3 implementation

Logic Utilization	Used	Available	Utilization
Number Of Slices	19	768	2%
Number of Slice Flip Flops	11	1536	0%
Number of 4 input LUTs	35	1536	2%
Number of bonded IOBs	17	124	13%
Number of GCLKs	1	8	12%

6 SIMULATION RESULTS

The state diagram design is simulated using Xilinx stateCAD (State Bench Simulator) for different floors. In 2nd lock, PB2 is active state change to MU2 state and out put HBRG “01”is generated which moves the motor upward direction as shown in Fig. 6. When elevator car reached at floor 2, in the 4th clock, S2 will be active(high), sate will change to F2 state and at this state output is HBRG”00” means motor stop and FLOOR “10” shown 02 which is input to seven segment display. In the same manner the elevator moving upward and downward between three floors is shown in Fig. 7 and Fig. 8.

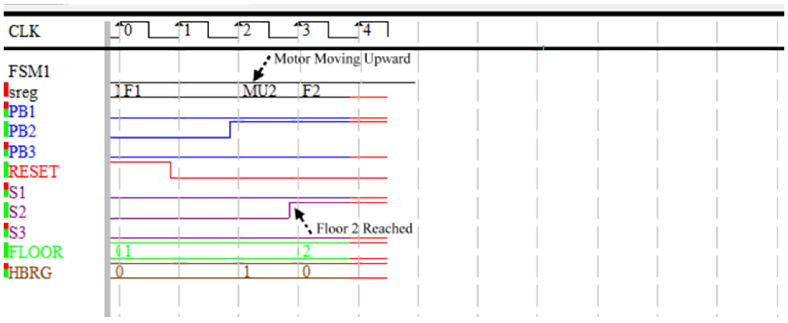

Fig. 6. Elevator moving upward for floor 2

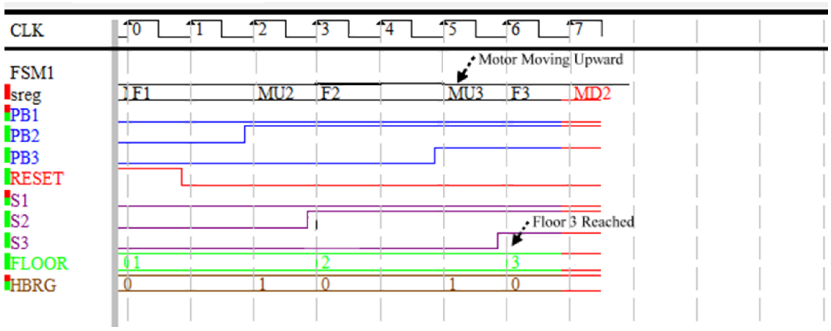

Fig. 7. Elevator moving upward for floor 3

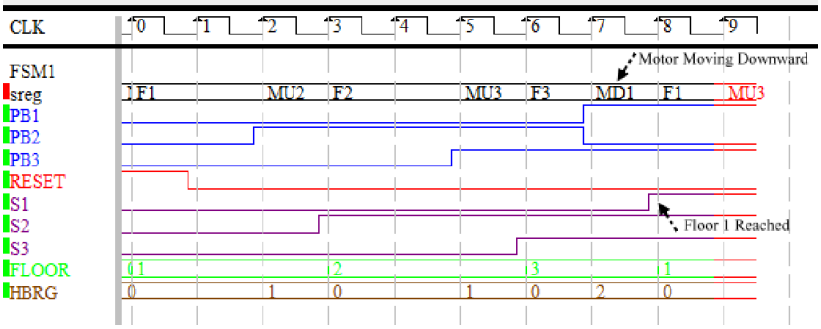

Fig. 8. Elevator moving downward for floor 1

7 CONCLUSIONS

The FPGA based elevator control system provides more flexibility, compatible than Microcontroller PLC based control system in which handwritten programming is used. In this way embedded system engineer can design a control system after a lot of process and errors that are comes in handwritten HDL programming. The designed elevator control system is implemented using finite state machine mechanism using Xilinx StateCAD tool that allows designer to change system without text oriented and errors prone rules in a time saving manner. Simulations have shown that this technique is quite promising. Reconfiguration possibilities of FPGA based control system by software and high speed due to parallel processing enhance productivity and reduce system development cost.

REFERENCES

[1] P. Rajesh, "Design and Implementation of Embedded Based elevator Control System," M Tech thesis, 2010.

[2] National Instruments, *PACs for Industrial Control, the Future of Control*, 2006. [Online] Available: http://zone.ni.com/devzone/cda/tut/p/id/3755 (Feb. 1, 2006)

[3] S. Ichikawa, M. Akinaka, R. Ikeda, H. Yamamoto, "Converting PLC Instruction Sequence into Logic Circuit: a Preliminary Study," *IEEE International Symposium on Industrial Electronics*, pp. 2930-2935, 2006.

[4] J. J. Rodriguez-Andina, M. J. Moure and M. D. Valdes, "Features, Design Tools and Application Domains of FPGAs," *IEEE Trans. On Industrial Electronics,* vol. 54, no. 4, pp. 1810-1823, Aug. 2007.

[5] K. D. Muller, G. Frick, E. Sax, M. Kuhl, "Multiparadigm Modeling in Embedded System Design," *IEEE Transections on Control System Technology*, vol. 12, no. 2, pp. 279-292, 2004.

[6] J. Becker, G. Hettich, R. Constapel, J. Eisemann, J. Luka, "Dynamic and Partial FPGA Exploitation," in *Proceedings of IEEE*, vol. 95, no. 2, February 2007.

[7] S. K. Wood, D. H. Akehurst, O. Uzenkov, W. G. J. Howells, and K. D. A. McDonald-Maier, " A Model-Driven Development Approach to Mapping UML State Diagrams to Synthesizable VHDL," *IEEE Transection on Computers*, vol. 57, 10, pp. 1357-1371, 2008.

[8] R. Nuss, *A New Paradigm for Synchronous State Machine Design in Verilog*, 1999. [Online] Available: http://www.ideaconsulting.com 1999.