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Design and Performance Analysis of 1 bit Full Adder in Subthreshold Region using 45nm Technology

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ABSTRACT: Full adder is the fundamental block of any digital system like microprocessor, microcontroller, DSP (Digital Signal Processing). In this paper a new architecture of full adder optimized under sub–threshold region is proposed. The newly proposed adder is based on modified multiplexer using GDI (Gate Diffusion input) and operated under sub-threshold region for low power consumption using 45nm Technology and analyzed with respect to power consumption, delay, Power Product Delay (PDP) and Energy Delay Product (EDP). The supply voltage is kept 200mV.

KEYWORDS: Full adder, GDI, Delay, PDP, EDP.

1 INTRODUCTION

Each and every microprocessor, digital signal processor (DSP),data processing application like specific integrated circuit (ASIC) contains the data path and the data path with its addressing unit which is made of arithmetic units, such as comparators, adders and multipliers. Binary addition is the most important operation found in the most arithmetic component [1]. 1-bit Full Adder is used for one bit binary addition. So if it is possible to enhance the performance of 1bit Full Adder it will enhance the overall performance.

For medical purpose, sensor networks, microcontroller, wireless computation low power devices are getting popular day by day. These devices need to be more energy efficient. Supply voltage scaling is the most effective way to meet the requirement. Reducing supply will reduce the power dissipation [2].Several design of full adder are used for several purpose. Every design has both advantage and disadvantage. So there is no ideal design. In this paper a newly proposed subthreshold adder is designed and analyzed its performance a according to delay, average power, PDP and EDP using 45 nm technology and the supply voltage is kept at 200mV.

2 POWER CONSUMPTION

The average power dissipation for a CMOS circuit is given by [3][4]:

$$P_{avg} = P_{dynamic} + P_{short\ circuit} + P_{static} \quad \text{.....(1)}$$

$$= V_{dd} . f_{clk} . \sum(V_{i\ swing} . C_{i\ load} . \alpha_i) + V_{dd} . \sum I_{i\ sc} + V_{dd} . I_l .$$

where f_{clk} is the system clock frequency, $V_{i\ swing}$ is the voltage swing at node *i* (ideally equal to V_{dd}), $C_{i\ load}$ is the load capacitance at node *I,* α_i is the activity factor at node *I*, and *Isc* and I_l are the short circuit and leakage currents, respectively. When operating CMOS device in the sub-threshold region, the power supply voltage is kept lower than the absolute of the

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devices' threshold voltage to make sure that the transistor channel is never fully inverted , but is operated in weak or moderate inversion while the transistor is its 'on' state[5]

3 TRUTH TABLE AND EQUATION

Usually a Full adder have three 1-bit input(A, B, Cin) and it has two output(Sum ,Carry).The expression of sum and carry out can be written as[3]

$$Sum = (A \text{ xor } B) \text{ xor } C$$

And $$Carry = AB + BC + CA$$

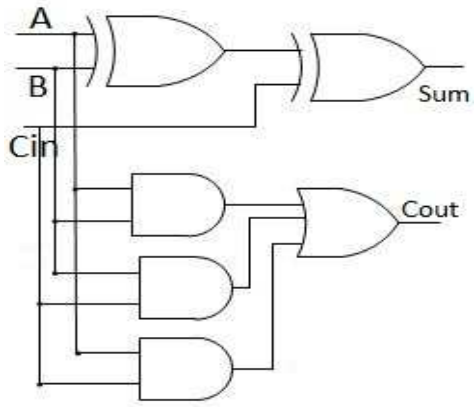

Fig. 1. Full Adder

3.1 GDI

- GDI(Gate Diffusion Input technique) -a new low power design technique is used to implement a wide range of complex logic function using only two transistor. This method is very suitable for design of fast, low power circuits, using reducing number of transistors. Minimum number of transistor helps to reduce the area. The conventional CMOS and PTL technique have several problems like static power dissipation, unusual delay, long critical path. The GDI based design meet most of the issues[6][7].
- A GDI cell contains 3 input - G(common gate input of nMOS and pMOS) ,P(input to the source/drain of pMOS)ad N(input to the source / drain to the nMOS).Its an important thing that not all the functions are possible in standard p-well CMOS process, but can be successfully implemented in twin-well CMOS or SOI technologist. The given table below shows the input configuration of the GDI cell and their Boolean functions accordingly.

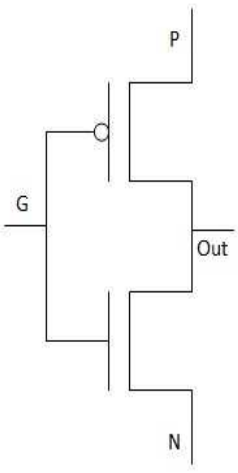

Fig. 2. Basic cell with GDI technique

Table 1. GDI truth table and operation

P	G	N	OUT	FUNCTION
B	A	Low	A 'B	F1
High	A	B	A'+ B	F2
B	A	High	A + B	OR
Low	A	B	AB	AND
B	A	C	A'B +AC	MUX
High	A	low	A'	NOT

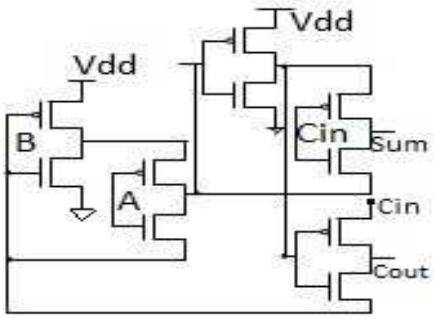

Fig. 3. GDI Full Adder[6]

3.2 14T

- It contains a 4T PTL XOR gate, an inverter and two transmission gates based multiplexer designs for sum and Carry out signals [8].

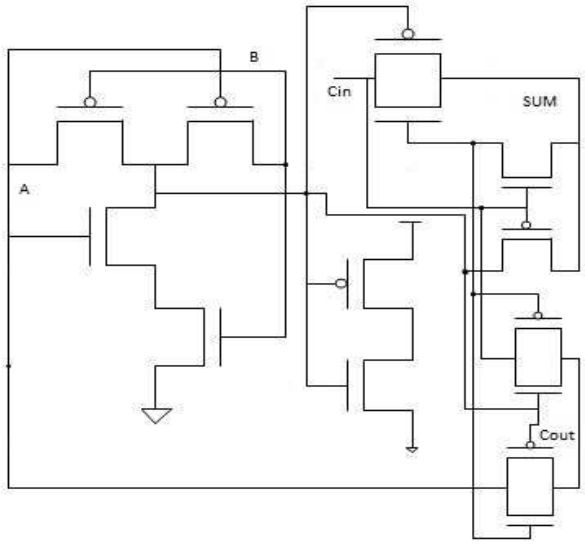

Fig. 4. 14 T Full Adder[6]

3.3 12T

- Six Multiplexers and 12 transistors are used to build a 12T design structure. Using pass transistor logic each Multiplexer is implemented with two transistors. There is no Vdd and Gnd connection in the circuit and there are some path containing three serried transistors. It increases the delay for the sum signal. The size of every transistor in mentioned path should be three times larger to balance the output and optimize the circuit for PDP.As a result the area is increased [9][6].

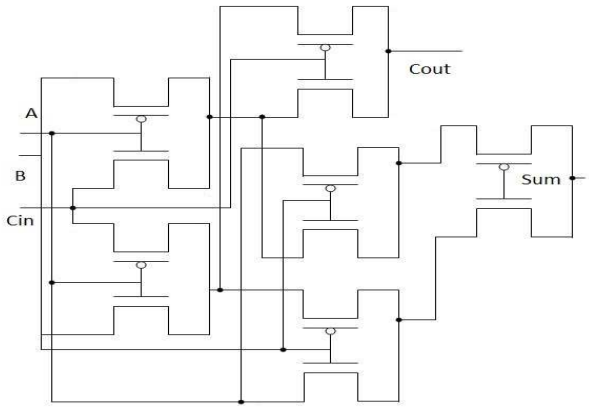

Fig. 5. 12 T Full Adder[6]

3.4 TRANSMISSION GATE FULL ADDER

- 20T transmission produces buffered outputs of proper polarity for both sum and carry. In this circuit 2 inverters are followed by two transmission gates which act as 8T XOR. Similarly 8T XNOR follows. It has 4 transistor XOR which is in the next stage is inverted to produce XNOR. These XOR and XNOR are used to produce SUM.

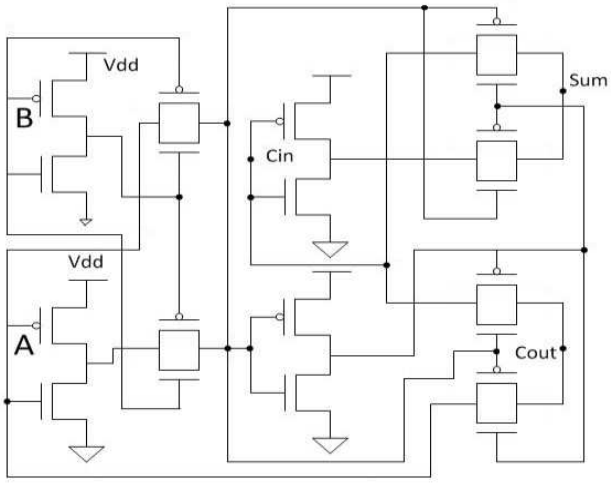

Fig. 6. Transmission Gate Full Adder[6]

3.5 PROPOSED DESIGN

- 18T are used in the design. 10 Transistors are used to make five 2-1 multiplexer. Among them four are used to generate Sum and one is used to generate Carry out. 4 transistors are used to invert A and B another 4 transistors are used to make AND and OR gate. All of the gates (except inverter) are designed with GDI technique where only two transistor are needed to construct any gate.

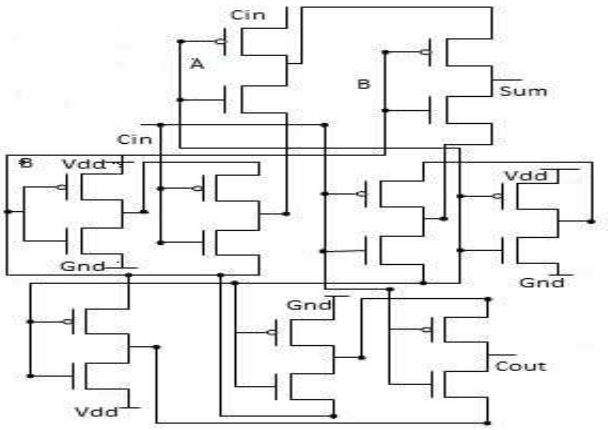

Fig. 7. Proposed Full Adder

4 RESULT

Full Adder has three input signal which are A,B Cin and two output signal Sum and Carry. The supply voltage is kept at 200mv and total simulation runs for 80 ns. Where Vdd= 200 mv. PDP=Power Delay Product, EDP=Energy Delay Product.

Adder	Average power(nW)	Delay (ns)	PDP (aJ)	EDP (10^{-26})
GDI	3.79	2.84	10.8	3.07
12t	42.5	4.85	235	99.9
14t	7.58	3.11	23.5	7.31
Transmission Gate	23.5	4.76	112	53.2
Proposed Adder	5.9	1.25	7.4	.931

Analysis shows that the propagation delay and the average power is significantly higher for 12T adder. As a result The EDP and PDP are also higher for this design. The Transmission gate adder has also relatively high average power consumption. It has got almost 50 percent of the EDP 12 T .Now among GDI, 14T, and Proposed design it is seen that the GDI has Got the minimum Average power(3.79nW) where as the proposed design has 5.9 nW but the delay of proposed adder has the minimum delay(1.23ns) which is less than the half of the delay(2.84ns) of GDI adder. Now As we know that the EDP and the PDP depends on the propagation delay and proposed design got the minimum delay so of course it has got the minimum EDP (.931*10^{-26}) and PDP(7.4 aJ). The average power of proposed adder is little high due to the extra 8 transistor than GDI but has low delay because of small critical path. Though the proposed design is GDI based it is more efficient than GDI adder because of its topology. It is based on multiplexer which makes it faster enough. The EDP of it is almost one third than GDI. All the simulation is done at room temperature 300K.

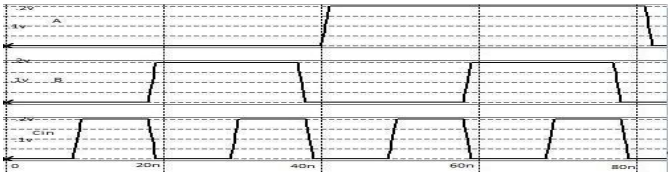

Fig. 8. The applied input signal (A,B,Cin)

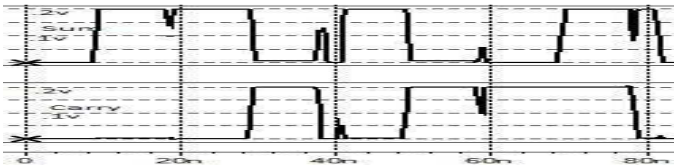

Fig. 9. Output of 14T Adder

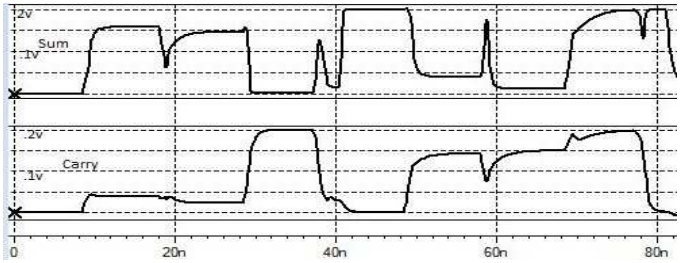

Fig. 10. Output of 12T adder

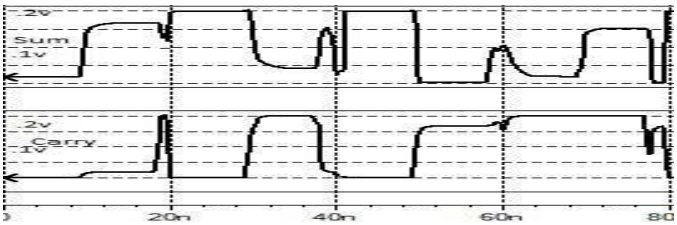

Fig. 11. Output of GDI based Full Adder

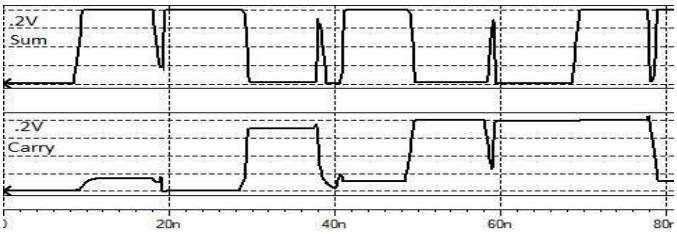

Fig. 12. Output of Transmission Gate Full Adder

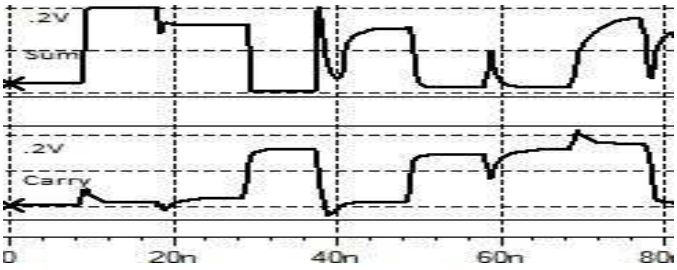

Fig. 13. Output of Proposed Adder

Fig. 14. Propagation delay

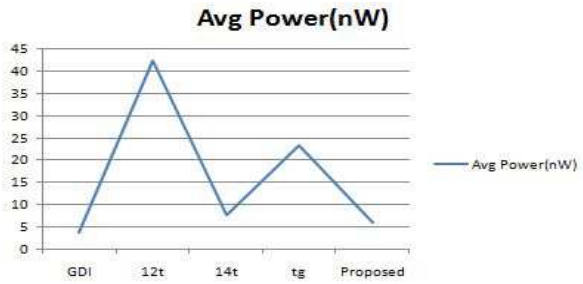

Fig. 15. Average Power

5 CONCLUSION

In this paper, an adder based on modified multiplexer using GDI is proposed which is under subthreshold region and analyzed its performance with respect to delay, power consumption, PDP and EDP. Compared to other reported results, power consumption and delay are reduced in 45nm technology.

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