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RTPG BASED BUILT IN SELF TEST FOR TEST COMPRESSION

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ABSTRACT: Built In Self Test (BIST) is used to test the working functions of IC circuit and it is one of the merit in IC's to check all the working functions inside the IC circuit. And one of the other cons of BIST is it does not need any other additional device or circuit to test the functions of IC as it has additional power and additional circuit than other devices. Thus BIST reduces the power consumption of addition circuit by consuming considerable power. There is no solution to overcome the problem of consumption of larger power even there are vast methods to reduce consumption of power. But one of the best existing power reduction method in BIST is PRPG, as it gives pseudo Random patterns to test. But it also produce considerable power consumption due to toggling and repetition of patterns. Therefore we can use RTPG to overcome the drawbacks of toggling and repetition in PRPG. RTPG is the Random Test Pattern Generator uses Multiple in Input Signature Register (MIST) in order to reduce the repetition. So the power consumption can be reduced by reducing the pattern in our proposed system.

KEYWORDS: BIST (Built In Self Test), PRPG, Multiple in input Signature Register, Design For Testability (DFT), RTPG, VLSI chips.

INTRODUCTION

Invention of transistor was the driving factor of growth in the Very Large Scale Integration (VLSI) technology. Integrated circuit is the circuit in which all the passive and active components are fabricated into a single chip. Initially the integrated chip could accommodate only a few components. As the days passed, the device become more complex and require more number of circuits which made the device look bulky. Instead of accommodating more circuits in the system, an integration technology was developed to increase the number of components that are to be placed on a single chip. This technology not only helped to reduce the size of the device but also improved their speed.

Tests are applied at several steps in the hardware manufacturing flow and for certain products, may also be used for hardware maintenance in the customer's environment. The tests are generally driven by test programs that execute using automatic test equipment (ATE) or, in the case of system maintenance, inside the assembled system itself. In addition to finding and indicating the presence of defects (i.e., the test fails), tests may be able to log diagnostic information about the nature of the encountered test fails. The diagnostic information can be used to locate the source of the failure.

It is really difficult to test digital circuits as a bulky amount of test data have to be delivered to the circuit under test (CUT). It is more difficult to test VLSI chips, because of their complicated functionality and size caused by increased integration levels of VLSI chips. Testing of VLSI chips are expensive. The two important factors to contribute the test cost are the test data volume and test power.

EXISTING SYSTEM

Built-In-Self-test (BIST) is a design-for-test (DFT) methodology in which the testing logic to detect faulty chips is built inside the chip. BIST possess reduced test development time, low test application time, eliminating the need for high-speed

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hardware testers, provision for at-speed tests, in-field test capability, and high fault coverage. Power dissipation during scan-based tests is higher than the normal operation of the circuit due to increased switching activity. Power dissipation during scan-based tests is higher than the normal operation of the circuit due to increased switching activity.

DISADVANTAGES OF EXISTING SYSTEM

- It consumes high power
- Repetition of patterns in the test
- Pattern is not checked before processing
- Slower fault detection
- Low quality testing

PROPOSED SYSTEM

A new technique is applied to get low shift power RTPG to improve the trade-off between test coverage loss and shift power reduction in logic. To get the required tradeoff, an additional hardware module named transition controller is implemented by which the adjacent test vector's correlation is increased. To calculate the power consumption during scanning, weighted transition by adjacent test patterns is selected. During shift mode the previous test responses in scan flip flops are given as feedback to a transition controller which is capable of generating highly correlated test patterns so that the switching activity will reduce.

BLOCK DIAGRAM

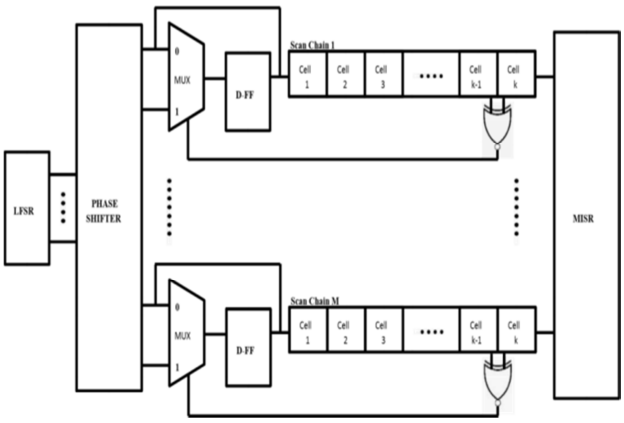

Fig. 1 Block Diagram

LINEAR FEEDBACK SHIFT REGISTER

The XOR gate provides feedback to the register that shifts bits from left to right. The maximal sequence consists of every possible state except the "0000" state is called linear-feedback shift register (LFSR). A linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is XOR. Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value.

The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. An LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle.

The function is an affine map, not strictly a linear map, but it results in an equivalent polynomial counter whose state is the complement of the state of an LFSR. A state with all ones is illegal when using an XNOR feedback, in the same way as a state with all zeroes is illegal when using XOR. This state is considered illegal because the counter would remain "locked-up" in this state. The sequence of numbers generated by an LFSR or its XNOR counter part can be considered a binary numeral system just as valid as Gray code or the natural binary code. The arrangement of taps for feedback in an LFSR can be expressed infinite field arithmetic as apolynomialmod2. This means that the coefficients of the polynomial must be 1's or 0's. This is called the feedback polynomial or reciprocal characteristic polynomial.

LFSR can be implemented in hardware, and this makes them useful in applications that require very fast generation of a pseudo-random sequence, such as direct-sequence spread spectrum. LFSRs have also been used for generating an approximation of white noise in various programmable sound generators.

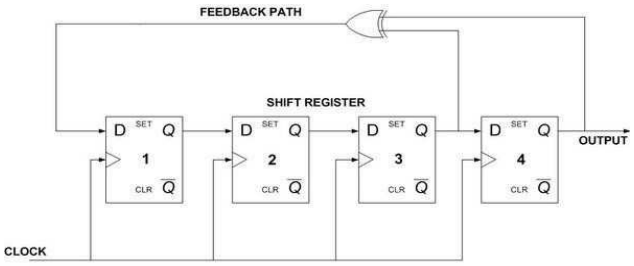

Fig. 2 Linear Feedback Shift Register

PHASE SHIFTER

Phase shifters are used to change the transmission phase angle of a network. Ideal phase shifters provide low insertion loss, and equal amplitude (or loss) in all phase states. While the loss of a phase shifter is often overcome using an amplifier stage, the less loss, the less power that is needed to overcome it. Most phase shifters are reciprocal networks, meaning that they work effectively on signals passing in either direction. Phase shifters can be controlled electrically, magnetically or mechanically. Most of the phase shifters described on this web site is passive reciprocal networks; we will concentrate mainly on those that are electrically controlled.

While the applications of microwave phase shifters are numerous, perhaps the most important application is within a phased array antenna system (a.k.a. electrically steerable array, or ESA), in which the phase of a large number of radiating elements are controlled to force the electro-magnetic wave to add up at a particular angle to the array.

SCAN CHAIN

Scan chain is a technique used in design for testing. The objective is to make testing easier by providing a simple way to set and observe every flip flop in an IC. The basic structure of scan includes the following set of signals in order to control and observe the scan mechanism. Scan-in and scan-out define the input and output of a scan chain. In a full scan mode usually each input drives only one chain and scan out observe one as well. A scan enable pin is a special signal that is added to a design. When this signal is asserted, every flip-flop in the design is connected into a long shift register.

Clock signal which is used for controlling all the FFs in the chain during shift phase and the capture phase. An arbitrary pattern can be entered into the chain of flip-flops, and the state of every flip-flop can be read out. In a full scan design, automatic test pattern generation (ATPG) is particularly simple. No sequential pattern generation is required - combinatorial tests, which are much easier to generate, will suffice. If we have a combinatorial test, it can be easily applied. Assert scan mode, and set up the desired inputs.

De-assert scan mode, and apply one clock. Now the results of the test are captured in the target flip-flops. Re-assert scan mode, and see if the combinatorial test passed. In a chip that does not have a full scan design i.e., the chip has sequential circuits, such as memory elements that are not part of the scan chain, sequential pattern generation is required. Test pattern generation for sequential circuits searches for a sequence of vectors to detect a particular fault through the space of all possible vector sequences.

Even a simple stuck-at fault requires a sequence of vectors for detection in a sequential circuit. Also, due to the presence of memory elements, the controllability and observability of the internal signals in a sequential circuit are in general much

more difficult than those in a combinational logic circuit. These factors make the complexity of sequential ATPG much higher than that of combinational ATPG.

MULTIPLE INPUT SIGNAL REGISTER

A serial-input signature register can only be used to test logic with a single output. We can extend the idea of a serial-input signature register to the multiple-input signature register (MISR). There are several ways to connect the inputs to both types (type 1 and type 2) of LFSRs to form an MISR. Since the XOR operation is linear and associative, so that (A B) C = A (B C), as long as the result of the additions are the same then the different representations are equivalent. If we have an n - bit long MISR we can accommodate up to n inputs to form the signature. If we use m < n inputs we do not need the extra XOR gates in the last n – m positions of the MISR.

Multiple-input signature register (MISR). This MISR is formed from the type 2 LFSR (with P*(x) = 1 2 3) by adding XOR gates xor_i1, xor_i2, and xor_i3. This 3-bit MISR can form a signature from logic with three outputs. If we only need to test two outputs then we do not need XOR gate, xor_i3, corresponding to input.

There are several types of BIST architecture based on the MISR. By including extra logic we can reconfigure an MISR to be an LFSR or a signature register; this is called a built-in logic block observer (BILBO). By including the logic that we wish to test in the feedback path of an MISR, we can construct circular BIST structures. One of these is known as the circular self-test path (CSTP).

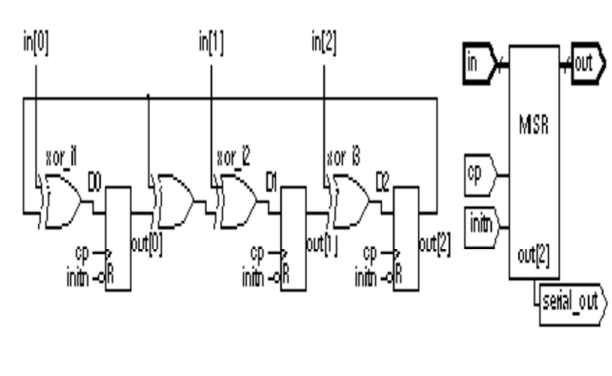

Fig. 3 Multiple Input Signal Register

We can test compiled blocks including RAM, ROM, and data path elements using an LFSR generator and a MISR. To generate all 2 n address values for a RAM or ROM we can modify the LFSR feedback path to force entrance and exit from the all-zeros state. This is known as a complete LFSR. The pattern generator does not have to be an LFSR or exhaustive.

SCAN CELLS IN RTPG

In normal RTPG the test vectors generated is passing directly to the scan chains which results in high switching activity. In our work, we have included a transition controller by which the adjacent test vector's correlation is increased. Scan cells in RTPG is used to test the cells in the chip which are working in a prescribed manner. Each scan cells denotes the gates in the chip. This cells are checked through the inputs from the linear feedback shift register. Between each scan cell, shift registers are used to shift the input.

FAULT COVERAGE

A fault represents the defect existing in a physical condition, which causes a circuit to fail to perform in a desired manner. A test vector is an input pattern that can produce a different output response in a faulty circuit from that of the fault-free circuit. Structural testing cannot guarantee detection of all possible manufacturing defects, as the test vectors are generated based on specific fault models.

Fault models provide a quantitative measure of the fault-detection capabilities of a given set of test vectors for a targeted fault model and this measure is called fault coverage and is defined as:

$$\text{Fault coverage} = \frac{\text{Detected faults}}{\text{Total faults}}$$

The test result obtained from Cadence Encounter Test and Diagnostics tool consists of two types of test coverage (fault coverage), i.e., test coverage (T_{cov}) and adjusted test coverage (A_{Tcov}) and are defined as:

$$AT_{COV} = \frac{\text{\# Tested faults}}{\text{\# Total faults} - \text{Redundant faults}}$$

Redundant faults does not deviate the functionality of the circuit and this faults cannot be detected by any test vector. Therefore it can be removed from the circuit by optimization. So AT_{Cov} is more useful in practice because it holds in consideration that redundant faults can be expressed in more than one form, so the measure is more accurate.

TRANSISTION CONTROLLER

The transition controller composed of a multiplexer, a XNOR gate and a D-flip-flop. The inputs of the XNOR gate is driven by the outputs of last two scan cells in the same scan chain, SC_{k-1} and SC_k. The output of the XNOR gate connects to multiplexer select input. To simplify discussion assume that there is no inversion between SC_k and SC_{k-1}. When SC_k and SC_{k-1} have different values, the value implied at the XNOR gate output is 0 and it causes the D-FF hold its previous value. Otherwise, the DFF will be updated by the phase shifter output. The value changes based on the last two cells as it is different it gives previous value, otherwise the same value is given as the input.

IMPLEMENTATION OF ADAPTIVE LOW POWER RTPG

Adaptive low power RTPG is used for shift power reduction in basic BIST (Built In Self Test). The implementation steps for low power RTPG are:

Step1: Generate scan chain for ISCAS'89 circuits by applying DFT constraints.

Step2: Generate netlist and ATPG files for the CUT.

Step3: Find out the Test Coverage and generate test pattern the Benchmark circuits without transition controller.

Step4: Modify the netlist to incorporate the Transition Controller circuit and find out the Test Coverage and generate test patterns of the benchmark circuits.

Step5: Determine the WTM.

IMPLEMENTATION AND RESULT

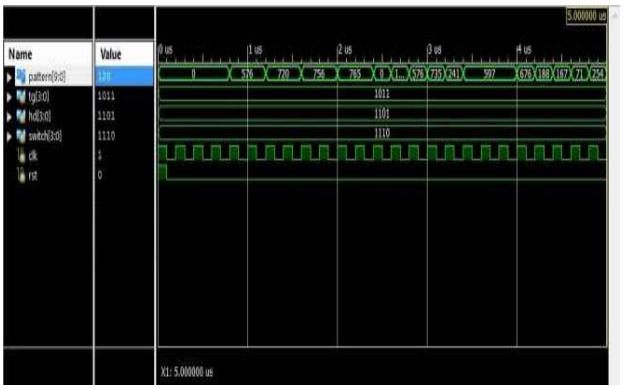

Fig. 4 output of the RTPG based test compression

The figure shows the output of the RTPG based test compression .the pattern which are generated is implemented through checking MISR circuit. The output is checked for repetition in certain clock pulses and the repetition are neglected. The pattern which are generated before the checking is neglected in the final generation of pattern which are represented in the figure as dots.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	68	20,480	1%	
Number of 4 input LUTs	41	20,480	1%	
Number of occupied Slices	44	10,240	1%	
Number of Slices containing only related logic	44	44	100%	
Number of Slices containing unrelated logic	0	44	0%	
Total Number of 4 input LUTs	41	20,480	1%	
Number used as logic	31			
Number used as Shift registers	10			
Number of bonded IOBs	12	320	3%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Average Fanout of Non-Clock Nets	2.63			

Fig. 5 device utilization in RTPG

The above figure shows the device utilization in RTPG. The device utilization is low compared to the existing system. The existing system will use 61 number of LUTs for the process. The proposed will use 41 LUTs instead of 61.this shows that the proposed system consumes very low utilization than the existing system. Thus the power consumption is lower than the existing system.

Fig. 6 power consumption of the proposed system

This shows that the power consumption of the proposed system. The proposed system will consumes the power of 0.336.the power in this is small compared to the existing system. The existing will consumes the power of 0.338 which is higher than the proposed system. So the proposed system is very efficient than the all other existing system.

CONCLUSION AND FUTURE WORK

In this paper, lower test power in shift mode is achieved by introducing a transition controller module which is capable of generating highly correlated test vectors depending upon the previous switching activities in the scan chain during shift mode. The architecture improves the trade-off between test coverage and shift power. Shift power is reduced considerably with a negligible test coverage loss so that the high power dissipation effects in CUT can be reduced. Since the transition controller covers a negligible portion of chip area, the burden of area overhead can be avoided. RTPG is implemented instead of PRPG. This reduces the power consumption and repetition of test patterns. This reduction in repetition allows low time consumption and reduced system complexity. RTPG is the Random Test Pattern Generator which is used to reduce the repetition by using Multiple Input Signature Register (MISR). MISR avoids repetition of patterns. RTPG achieves the shift

power ranges from 37.2% to 47.6% for the given circuit with small area penalty. By reducing the test pattern the power consumption is reduced. Thus by using our proposed system the power consumption is reduced.

In this project, the repeated patterns are reduced by using MISR which compares the previous test patterns and produced test pattern for certain cycles. In the scan chain toggling and repetitions can be reduced by using algorithms. Though it reduces the repeated patterns there is also repetition for a maximum of two or three times which is not able to be avoided so the power consumption for this pattern is unavoidable. So in future work, the repetition of the maximum two should be avoided so that the power consumption for this pattern is reduced considerably. Though it reduces power consumption of additional circuit it also consumes considerable power. Hence, in future a suitable circuit can be designed to reduce the power consumption to very low level.

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