International Journal of Innovation and Scientific Research
ISSN 2351-8014 Vol. 8 No. 2 Sep. 2014, pp. 136-146

http://www.ijisr.issr-journals.org/

Performance Comparison in Hybrid H- Bridge Multilevel inverter for Various PWM Strategies

***P. Satheesh Kumar*[1], *Dr. S.P. Natarajan*[2], *Dr. Alamelu Nachiappan*[3], *and Dr. B. Shanthi*[4]**

[1]Associate professor, Department of EEE,
Mailam Engineering College, Mailam,
Tamilnadu, India

[2]Professor & Head, Department of Instrumentation Engineering,
Annamalai University, Annamalai Nagar,
Tamilnadu, India

[3]Professor, Department of EEE,
Pondicherry Engineering College,
Pondicherry, India

[4]Professor, Centralized Instrumentation and Service Laboratory,
Annamalai University, Annamalai Nagar,
Tamilnadu, India

ABSTRACT: In this paper nine level Hybrid H- Bridge Multilevel inverter is analyzed for the various multi-carrier Pulse Width Modulation strategies. For the same nine level inverter output this particular topology has reduced count of switches, on comparing with the conventional Cascaded H Bridge Multilevel Inverter. For a single phase, nine level inverter output this topology requires one H-bridge and a half Bridge cell with Four equal voltage sources. Instead of sixteen controlled switches as in conventional method, this topology requires only twelve switches to obtain nine level output. The reductions in components count lowers, cost and complexities. Performance parameters have been analyzed for the nine level Hybrid H Bridge Multilevel inverter.

KEYWORDS: Alternate phase opposition disposition, Hybrid H-Bridge Multilevel Inverter, phase disposition, phase opposition disposition, phase shift pulse width modulation, sinusoidal pulse width modulation.

1 INTRODUCTION

Multilevel inverter (MLI) has wide range of high-power applications and feeds demands in industries in recent years. The aptness of MLI attracts the hot researchers in the direction of renewable energy sources for its numerous benefits. As renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system of high power applications, MLI still gains further credit to its field. MLI can operate at high switching frequencies while producing lower order harmonic components.

A multilevel inverter is a power-electronic system that generates a desired output voltage by synthesizing several levels of dc input voltages. The main advantages of multilevel inverters are lower cost, higher performance, less electromagnetic interference, and lower harmonic content [1].The most common multilevel inverter topologies are the diode-clamped, flying-capacitor, and cascaded H-bridge inverters with separate dc voltage sources [2]. The diode clamped multilevel inverter topology, restricts the use of it to the high power range of operation. Moreover flying capacitor based multilevel inverter also exhibits a disadvantage including more number of capacitors [3].

In recent years, the cascaded H-bridge inverters have wide applications. The merit includes modularity and the ability to operate at higher voltage levels and as the number of levels increases, the quality of the output signal will be improved. In addition inverter output voltage waveform will be closer to a sinusoidal waveform [4].

Moreover, high voltages can be managed at the dc and ac sides of the inverter, while each unit endures only a part of the total dc voltage. Needs of high number of semiconductor switches, involvement of separate DC source for each of H-bridge, voltage balancing issues are the notable drawbacks of cascaded H bridge inverter.

On comparing with the usual Cascaded H-Bridge multilevel inverters, for the same nine level output, this Hybrid H-Bridge multilevel inverter topology, the number of switches used reduced is only twelve switches. Therefore for this cost & simplicity reason, this multilevel inverter has some value of importance. Hence this paper focuses on applying various multi carrier based PWM techniques to this Hybrid H Bridge multilevel inverter to analyze and compare the various parameters like THD & V_{rms}.

2 HYBRID H-BRIDGE MULTILEVEL INVERTER TOPOLOGY DESCRIPTION

2.1 GENERAL STRUCTURE

The Hybrid H-Bridge Multilevel Inverter proposed in this paper is shown in Fig. 1. The cascaded half-bridges and full-bridge inverters are involved to form Hybrid H-Bridge Multilevel Inverter. The cascaded half-bridges produced dc voltage as output which is connected to full-bridge as DC input. Each half-bridge can make the DC source to be implicating into the voltage producing or to be bypassed. Therefore, by controlling of the cascaded half-bridges, the number of DC sources connected in the circuit will be changed, that leads to a variable DC voltage. To produce ac waveforms just alternate the direction of the dc voltage by using full bridge. Hence, the switching frequency of devices in the H-bridge equals to the base frequency of the desired ac voltage.

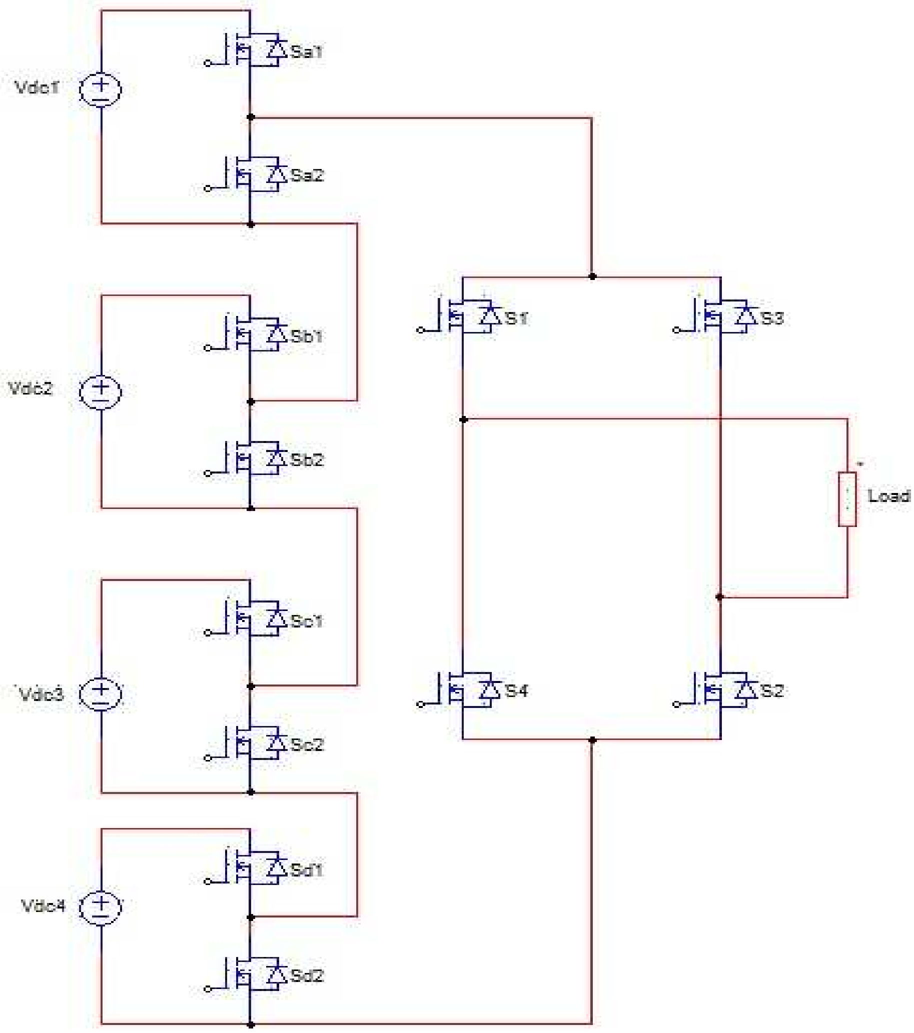

Fig. 1. 9-Level Hybrid H-Bridge Multilevel Inverter

Table 1. Switching Patterns for 9 levels Hybrid H-Bridge Multilevel Inverter

S. No	Multi conversion Cell		H-Bridge		Voltage levels
	On switches	Off switches	On switches	Off switches	
1	Sa1,Sb1, Sc1, Sd1	Sa2,Sb2, Sc2, Sd2	S1, S2	S3, S4	$+4V_{dc}$
2	Sa2,Sb1, Sc1, Sd1	Sa1,Sb2, Sc2, Sd2	S1, S2	S3, S4	$+3V_{dc}$
3	Sa2,Sb2, Sc1, Sd1	Sa1,Sb1, Sc2, Sd2	S1, S2	S3, S4	$+2V_{dc}$
4	Sa2,Sb2, Sc2, Sd1	Sa1,Sb1, Sc1, Sd2	S1, S2	S3, S4	$+1V_{dc}$
5	Sa2,Sb2, Sc2, Sd2	Sa1,Sb1, Sc1, Sd1	S1, S3	S2, S4	0
6	Sa2,Sb2, Sc2, Sd1	Sa1,Sb1, Sc1, Sd2	S3, S4	S1, S2	$-1V_{dc}$
7	Sa2,Sb2, Sc1, Sd1	Sa1,Sb1, Sc2, Sd2	S3, S4	S1, S2	$-2V_{dc}$
8	Sa2,Sb1, Sc1, Sd1	Sa1,Sb2, Sc2, Sd2	S3, S4	S1, S2	$-3V_{dc}$
9	Sa1,Sb1, Sc1, Sd1	Sa2,Sb2, Sc2, Sd2	S3, S4	S1, S2	$-4V_{dc}$

2.2 SWITCHING OPERATION

By turning on controlled switches S1 ,S2, (S3 and S4 turn off) the output voltage $+V_{dc}$ is produced across the load. Similarly turning on of switches S3, S4 (S1 & S2 turn off) $-V_{dc}$ output is produced across the load. Similarly turning on of switches S1, S3 (S2 & S4 turn off) Zero output is produced across the load. The above Table 1.clearly shows the switching patterns for 9 level of output

3 MULTIPLE CARRIER PULSE WIDTH MODULATION TECHNIQUES

In this PWM technique, more than one carrier wave which be either triangular or saw tooth wave form can be used. This paper focuses on various strategies.utilising more than one triangular wave as carrier and the reference wave is sinusoidal. Though there are many carrier wave arrangements, in this paper, the following four arrangements have been carried out. THD and V_{rms} values for these four strategies for various modulation indexes are compared.

3.1 Phase disposition PWM strategy.
3.2 Phase Opposition Disposition PWM strategy.
3.3 Alternate Phase Opposition Disposition PWM strategy
3.4 Phase Shift PWM strategy.

In these Multicarrier PWM schemes, several triangular carrier waves are compared with the single Sinusoidal reference wave. The number of carriers required to produce N level output is (m-1) where m is the number of carrier waveforms. The single sinusoidal reference waveform has peak to peak amplitude of A_m and a frequency f_m. The multiple triangular carrier waves are having same peak to peak amplitude A_c and same frequency $f_{c.}$ The single sinusoidal reference signal is continuously compared with all the carrier waveforms. A pulse is generated, whenever the single sinusoidal reference signal is greater than the carrier signal. The frequency ratio m_f is as follows: f_c / f_m

3.1 PHASE DISPOSITION PWM STRATEGY (PDPWM)

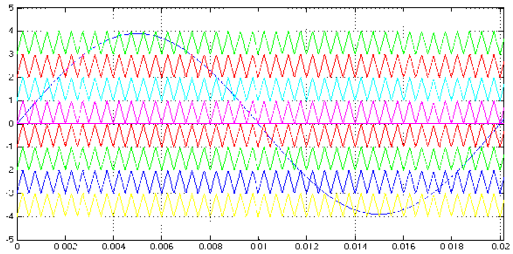

Fig. 2. Carrier arrangement for Phase Disposition PWM strategy

The above fig. 2 shows, Phase Disposition PWM strategy (PDPWM), where (m-1) carrier signal with the same frequency f_c and same amplitude A_c are positioned such that the bands they occupy are contiguous. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off.

Amplitude of modulation index for PDPWM is

$$m_{a} = 2A_{m} / (m-1) A_c$$

3.2 PHASE OPPOSITION DISPOSITION PWM STRATEGY (PODPWM)

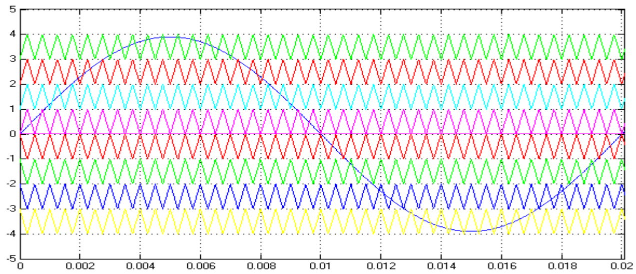

Fig.3. Carrier arrangement for Phase Opposition Disposition PWM strategy

POD PWM strategy is shown in fig.3, where the carrier waveforms, above the zero reference are in phase. The carrier waveforms below are also in phase, but are 180 degrees phase shifted from those above zero. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off.

Amplitude of modulation index for PODPWM is

$$m_{a} = 2A_m / (m-1)^* A_c$$

3.3 ALTERNATE PHASE OPPOSITION DISPOSITION PWM STRATEGY (APODWM)

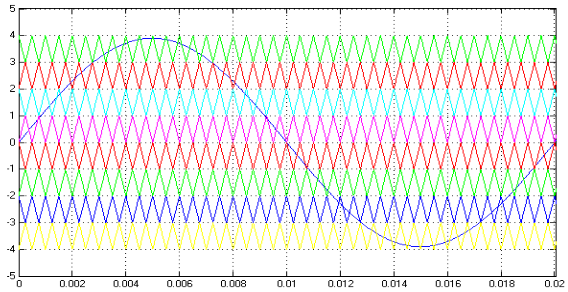

Fig. 4. Carrier arrangement for Alternate Phase Opposition Disposition PWM strategy

The above fig. 4 shows APOD strategy where the multiple carriers having same amplitude are phase displaced from each other by 180 degrees alternately. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off.

Amplitude of modulation index for PODPWM is

$m_{a} = 2A_m \ / (m-1)^* A_c$

3.4 PHASE SHIFT PWM STRATEGY (PSPWM)

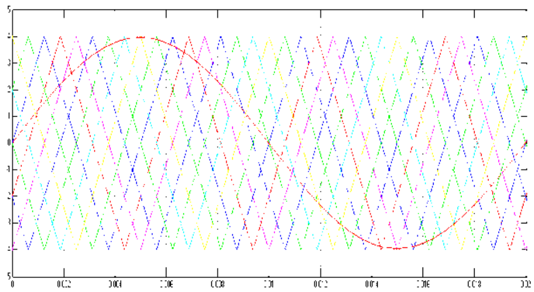

Fig. 5. Carrier arrangement for Phase shift PWM strategy

The above fig. 5 shows PSPWM strategy where the multiple carriers having the same amplitude and frequency which are shifted to one another by certain degrees decided by the No. of levels. Thus for nine level output, 8 triangular carrier waves which are phase shifted by 45 degrees is utilized .The reference waveform is single sinusoidal (i) for odd m_f the waveforms have odd symmetry resulting in even and odd harmonics and (ii) for even m_f , PSPWM waves have quarter wave symmetry resulting in odd harmonics only.

Amplitude of modulation index for PSPWM is

$$m_a = A_m / (A_c /2).$$

4 SIMULATION RESULTS

The fig. 6 shown below is the simulink model of the 9 –level Hybrid H Bridge Multilevel inverter using power system block set. The following parameter values are used for simulation: V_1 =100v, V_2 =100v, V_3 = 100v, V_4= 100v .Gating signals for Phase shifted carrier wave arrangement and three different, level shifted carrier wave arrangements are simulated.

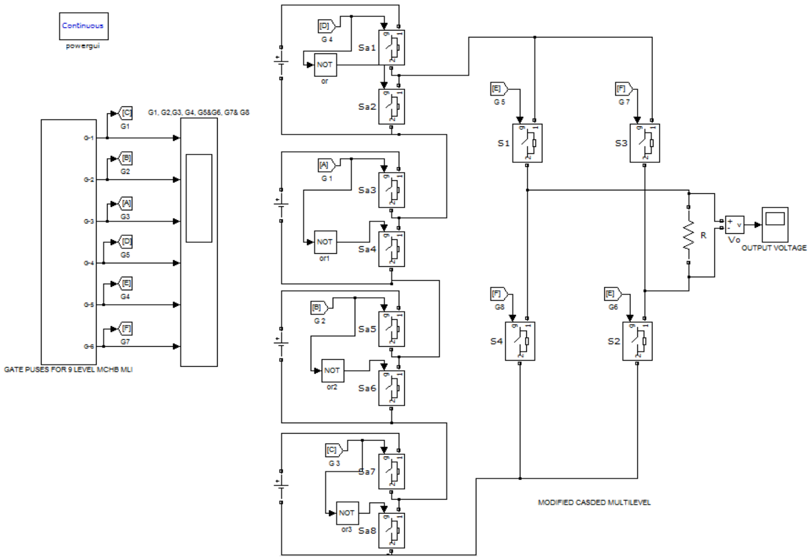

Fig. 6. Simulink Modeling of the Hybrid H-Bridge Multilevel Inverter

Simulations are done for various values of m_a and the corresponding THD% are observed using FFT block and listed in Table 2 The V_{rms} (fundamental) of the output voltage for various values of m_a and the corresponding Voltages are listed in Table3.The comparison of Vrms and THD is shown in fig 7 & 8.

Table 2. THD comparison

M_a	PD PWM	POD PWM	APOD PWM	PS PWM
1	13.55	13.25	13.12	12.9
0.9	16.62	16.59	16.51	16.25
0.8	16.93	16.68	17.11	16.17

Table 3. V_{rms} comparison

M_a	PD PWM	POD PWM	APOD PWM	PS PWM
1	399.9	401	399.8	400
0.9	359.8	359.7	359.8	360.2
0.8	319.9	319.6	319.9	319.9

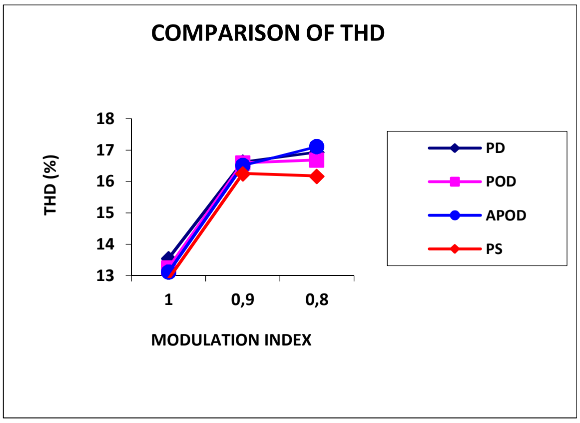

Fig. 7. Comparison of V_{rms}

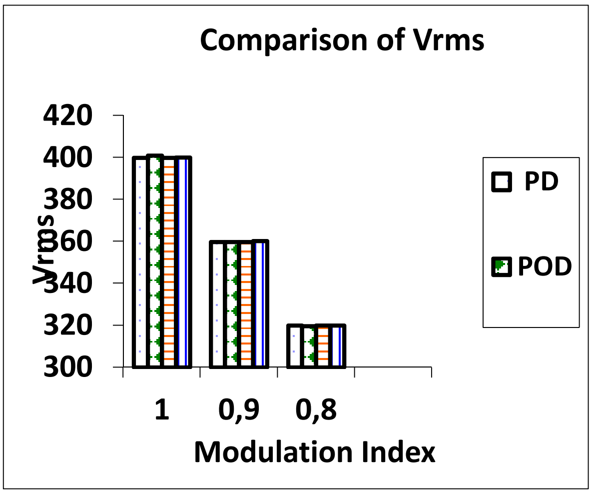

Fig. 8. Comparison of THD

The Simulated 9-level Output Voltage waveform of Hybrid H Bridge MLI using PDPWM Strategy is shown in fig. 9 and Fig. 10 shows the FFT plot of 9-level Hybrid H Bridge MLI using PDPWM Strategy. The Simulated 9-level Output Voltage waveform of Hybrid H Bridge MLI using PODPWM Strategy is shown in fig 11 and Fig: 12 shows the FFT plot of 9-level Hybrid H Bridge MLI using PDPWM Using PODPWM Strategy. The Simulated 9-level Output Voltage waveform of Hybrid H Bridge MLI using APODPWM Strategy is shown in fig 13 and Figure: 14 shows the FFT plot of 9-level Hybrid H Bridge MLI Using APDPWM using PODPWM Strategy. The Simulated 9-level Output Voltage waveform of Hybrid H Bridge MLI using PSPWM Strategy is shown in fig 15 and Fig: 16 shows the FFT plot of 9-level Hybrid H Bridge MLI using PSPWM Strategy.

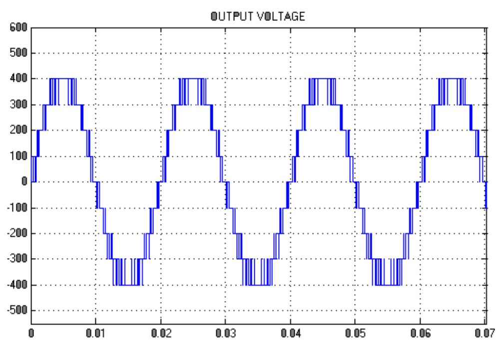

Fig.9. Simulated 9-level Output Voltage waveform of Hybrid H Bridge MLI Using PDPWM Strategy

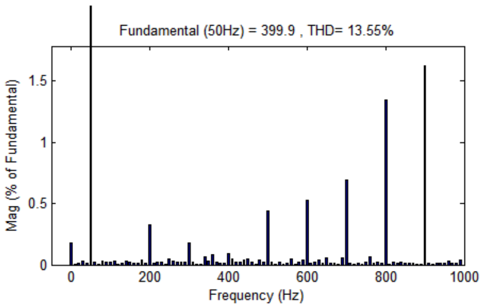

Fig. 10. FFT plot of 9-level Output Voltage waveformHybrid H Bridge MLI Using PDPWM Strategy

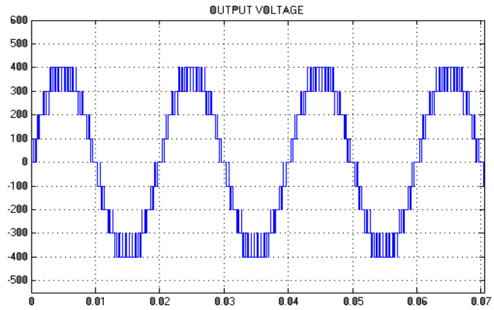

Fig .11. Simulated 9-level Output Voltage waveform of Hybrid H Bridge MLI Using PODPWM Strategy

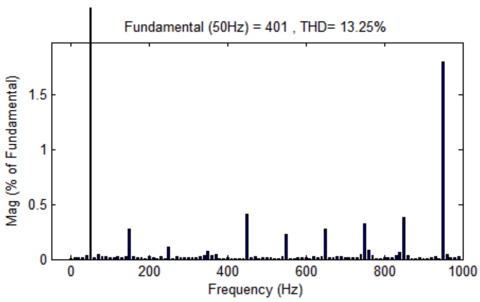

Fig. 12. FFT plot of Hybrid H Bridge MLI Using PODPWM Strategy

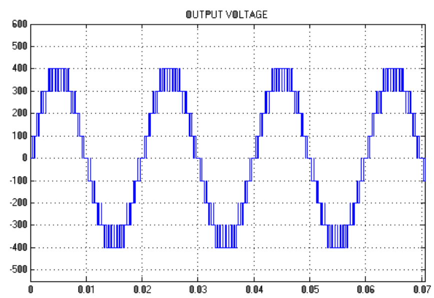

Fig .13. Simulated 9-level Output Voltage waveform of Hybrid H Bridge MLI Using APODPWM Strategy

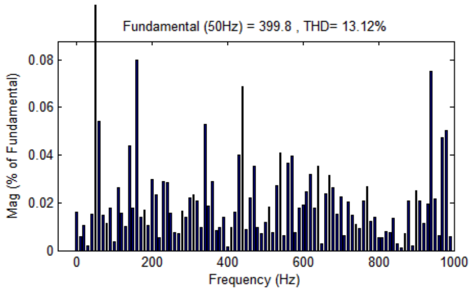

Fig. 14. FFT plot of Hybrid H Bridge MLI Using PODPWM Strategy

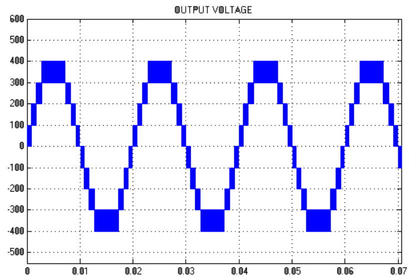

Fig. 15. Simulated 9-level Output Voltage waveform of Hybrid H Bridge MLI Using PSPWM Strategy

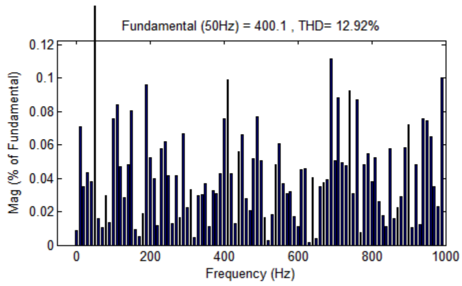

Fig. 16. FFT plot of 9-level Hybrid H Bridge MLI Using PSPWM Strategy

5 CONCLUSION

Hybrid H Bridge multilevel inverter has been analyzed for various multi carrier sinusoidal Pulse Width Modulation strategies. This topology has the credit of having only twelve switches, instead of 18 switches in the conventional plants, which support reduction in switching losses, cost and circuit complexity.

Performance factors like %THD and V_{RMS} have been measured, and analyzed for Phase shifted carrier wave arrangement and three different, level shifted carrier wave arrangements both applied to the Single phase nine levels Modified cascaded multilevel inverter. The values have been measured for various modulation indexes. It is found that the PDPWM strategy provides appreciable %THD and acceptable V_{RMS}. In addition, it is also observed that it has less number of dominant harmonics than the other strategies.

REFERENCES

[1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind.Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.*

[2] Z.Du, L.m.Tolbert, J.N.Chiasson, and B.Opineci, "A cascaded multilevel inverter using a single dc power source", in *Proc. IEEE APEC, pp.426-430, 2006.*

[3] Fang Zheng Peng "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", *IEEE Trans. Ind .Appl., Vol.37, No.2, March/April 2001.*

[4] J. I. Leon, R. Portillo, S. Vazquez, J. J. Padilla, L. G. Franquelo, and J.M. Carrasco, "Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters," *IEEE Trans.Ind. Electron., vol. 55, no. 9, pp. 3239–3248, Sep. 2008.*

[5] Y. Li and B. Wu, "A novel dc voltage detection technique in the chb inverter-based statcom," *IEEE Trans. Power Del., vol. 23, no. 3, pp.1613–1619, Jul. 2008.*

[6] J. Rodriguez, J. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron, vol.49, no. 4, pp. 724–738, Aug. 2002.*

[7] Ebrahim Babaei "A Cascaded Multilevel converter Topology With Reduced Number of Switches", IEEE Trans. Power Electron vol.23,no.6, Nov 2008.

[8] Rokan Ali Ahmed, S. Mekhilef, Hew Wooi Ping, ''New multilevel inverter topology with reduced number of switches'', Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10), Cairo University, Egypt, December 19-21, 2010, Paper ID 236.