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RF CMOS LNA Using Feed-forward Noise and Distortion Cancellation Topology

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ABSTRACT: An elegant CMOS LNA design using feed-forward noise and distortion cancellation technique is presented in this paper. The design is implemented in 130nm CMOS technology. In comparison to other conventional technique the proposed LNA shows improvement in performance parameter such as NF, gain, stability and power dissipation. . In this paper a CMOS inverter along with resistive negative feedback is used to provide necessary biasing and impedance matching at input port. The LNA design is inductorless and hence the size is small. Using this technique LNA shows a gain of 34-22 dB with a noise figure of 1.6-1.9dB for operating bandwidth of 600 MHz – 3GHz. The proposed LNA drains 13mA current from 1.2V power supply.

KEYWORDS: LNA, noise cancelling, low power, high gain, inductorless.

1 INTRODUCTION

With the expansion of wireless communication markets mobile handsets need to support as many as features available. Thus there is need of research work in the field of SDR, cognitive radio, WiMAX applications [1]-[4]. One of the major challenges in this sector is the noise and distortion which is the root cause of failure of the system. RF front end is the key important factor that satisfies all specifications requirement of communication channel [1]. RF front end has range of operating frequencies from 50MHz to several GHz [2]. Wideband LNA is commonly used for such high bandwidth operations. At higher frequencies Wideband LNA's suffer from intrinsic noise, mainly thermal noise. Thus various techniques have been developed to minimize the noise and improve LNA performance.

In this paper a feed-forward noise and distortion cancellation technique is proposed to improve the performance of wideband LNA by reducing noise and other unwanted signals. The critical performance parameters such gain, noise figure, third order intercept point (IIP3) and power dissipation improves drastically. Input Impedance matching is achieved by using negative resistive feedback along with feed-forward topology. It also improves stability of the system.

The proposed negative feedback and feed-forward noise-canceling operation principle is presented in Section II. Section III contains block diagram of the proposed design and brief explanation on its functionality. Section IV presents the RF CMOS LNA design schematics implemented in Agilent's ADS 2009 software. Results are shown in section V and finally, a conclusion is summarized in Section VI.

2 WIDEBAND LNA

In recent years various several techniques such as noise cancellation, capacitive feedback network [5], and other topologies are used to break the trade-off between noise figure F and wideband input impedance matching. Also for designing LNA certain optimization techniques for improving design performance and characteristics are mentioned in [6]. Noise figure F is one of the major characteristic for wideband amplifiers. F determines the sensitivity of the system. Lower the

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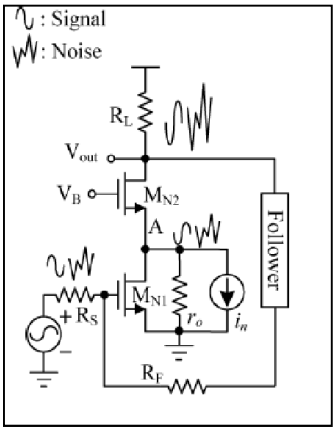
value of F higher will be its sensitivity. However, the input impedance matching for wideband LNA is not good enough as compared to narrow band LNA.

For wideband LNA shunt-shunt feedback can be used for input impedance matching and NF. Negative feedback decreases input impedance matching for common source amplifiers while positive feedback increases the impedance matching for common gate amplifiers. In noise cancelling technique, the key idea is to use an auxiliary amplifier for sensing the signal and noise voltages. By combining the outputs of an auxiliary amplifier and main amplifier to cancels the noise from the input device, adding to the signal strength from both amplifiers to output node.



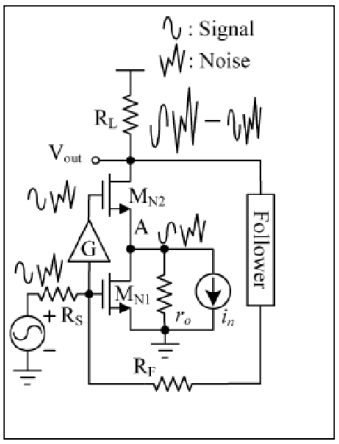


Fig. 1. Conventional resistive negative feedback. Fig. 2. Resistive feedback with noise cancellation technique

The above figures show a conventional feedback network in fig 1, while fig 2 shows feedback network with noise cancelling technique. In fig 1 M_{N1} is trans-conductance transistor and M_{N2} is a cascode transistor. M_{N2} is used to increase the output impedance and improves isolation between input and output ports. The current source i_n models the transistor M_{N1}. M_{N1} is the main source of thermal noise in the circuit.

M_{N1}, M_{N2}, R_L and follower circuit forms a common source inverse amplifier with high input impedance and low output impedance. RL is the resistive load connected at the output. The feedback resistor RF is given by

$$R_F = R_S (1+A_V)$$

Where,

R_S is the input source impedance,

A_V is the gain of the amplifier circuit.

In RF CMOS the input source resistance $R_S = 50\ \Omega$.

3 BLOCK DIAGRAM OF PROPOSED DESIGN

The block diagram consists of four main functional blocks namely matching n/w, stage I amplifier, noise cancelling model (adder circuit along with constant current) & stage II amplifier.

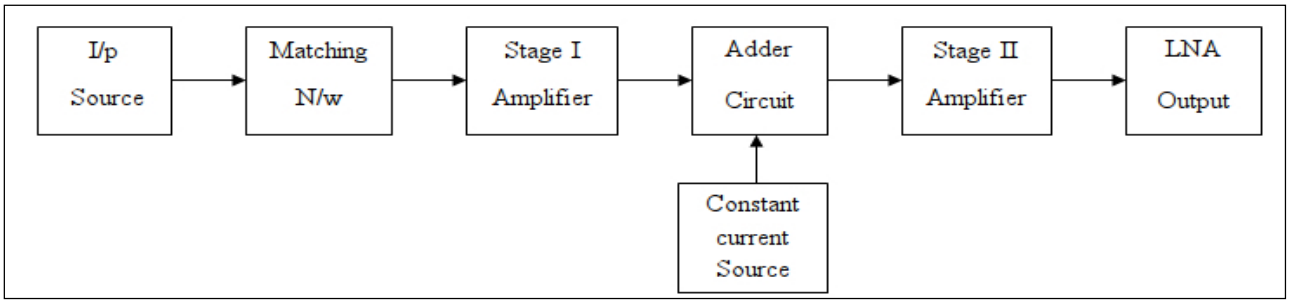


Fig. 3. Block Diagram of Proposed design

The proposed design implies CG topology. A CMOS inverter along with resistive feedback is implemented, which acts as self biased circuit. The resistive feedback provides necessary matching to input port. Therefore in this design conventional LC ladders are not used to provide impedance matching. In order to achieve high gain the design is implemented in II stages. Adder circuit is noise cancelling circuit which uses constant current source as high gain reference amplifier to cancel the noise from input signal. Thus by this approach a CMOS LNA can be designed which is suitable for various RF applications. The proposed design has operating bandwidth from 0.6GHz to 3GHz.

4 DESIGN SCHEMATICS

The fig 4 shows the schematic of proposed design implemented in Agilent's ADS 2009 software. The design is implemented in 0.13um technology. In this design M1, M2 transistor forms a CMOS inverter with a negative feedback resistor. Using this method M2 transistor will adapt the voltage level of M1 transistor and is called as self biasing. Transistor M2 is main source of intrinsic noise in the circuit. The output of CMOS inverter is given as input to transistor M5. Transistor M3 and M4 also form a CMOS inverter. It is used as second stage amplifier mainly to achieve higher gain. Transistor M5 and M6 is the noise cancelling circuit. The constant current source generates a reference signal which is given as input to transistor M6. The noise cancelling circuit will add the output from transistor M5 and M6 and thus will suppress noise from the original signal.

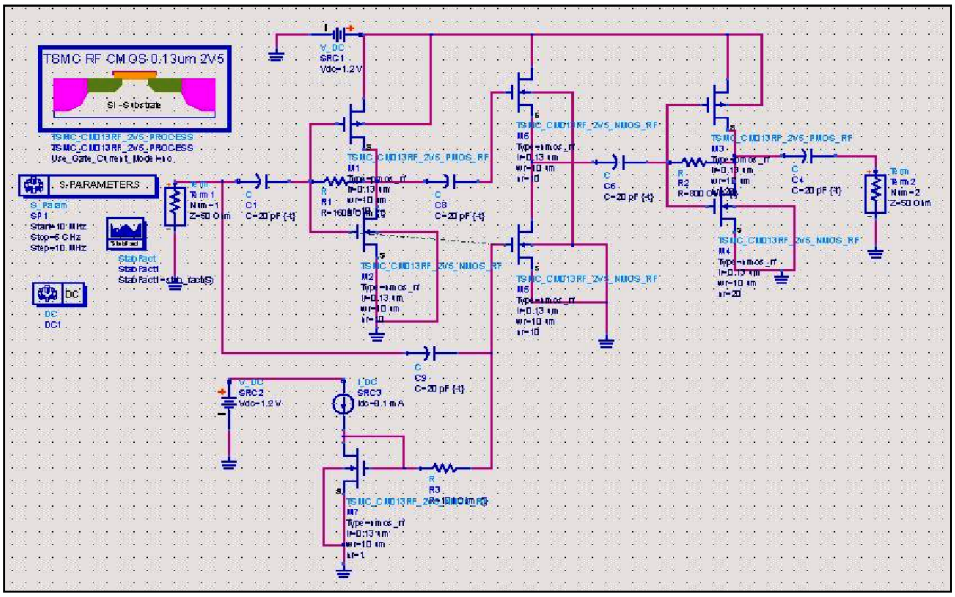


Fig. 4. Schematics of proposed LNA

5 RESULT AND DISCUSSION

In this section the results of the proposed designed are shown. This section discusses S- parameter results, i.e. S11, S12, S21, S22, Noise Figure and stability.

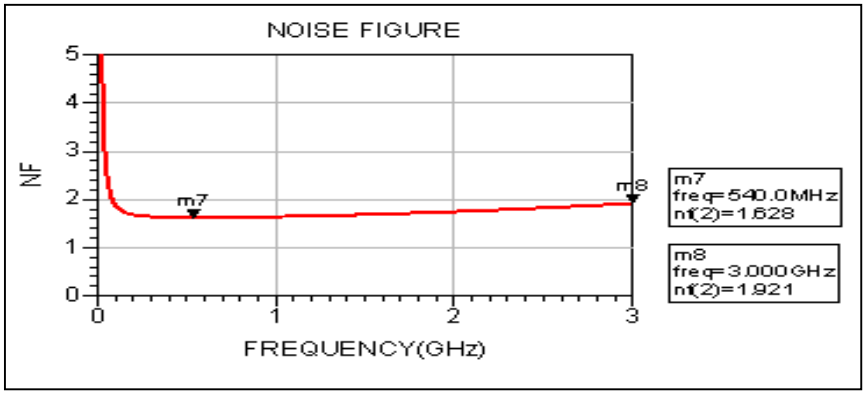


Fig. 5. Noise Figure over the operating frequency range

Fig 5 shows NF results. NF ranges from 1.6dB to 1.9dB for the overall operating bandwidth. Ideally, noise figure should be less than 3dB. The noise figure achieved is much less than 3dB. Also it can be seen that as the frequency increases NF also gets increased.

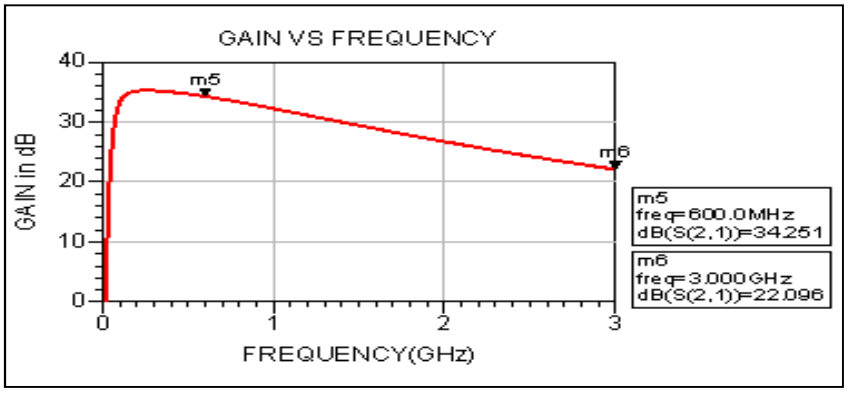


Fig. 6. Gain v/s frequency response

Fig 6 shows gain achieved by the proposed design. Gain of this system varies from 34dB at 600MHz to 22dB at 3GHz. For low noise amplifier gain should be as high but it degrades at higher frequencies. Therefore to achieve higher gain amplifiers are used in stages.

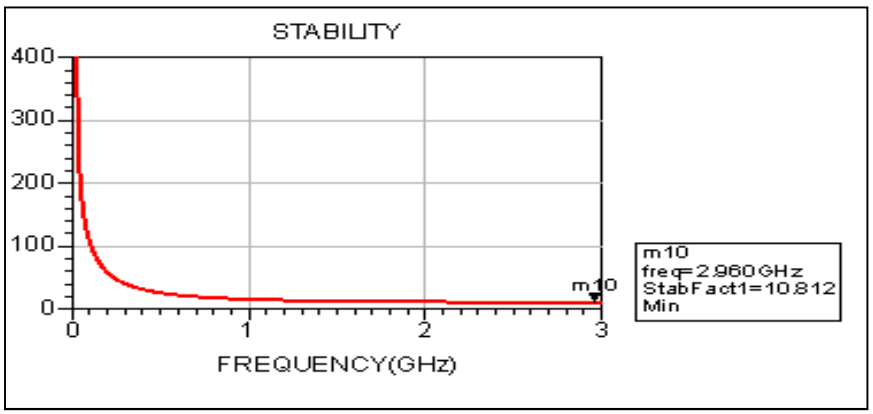


Fig. 7. Stability v/s frequency

Fig 7 shows stability of the system over the operating frequency range. For an LNA to be unconditionally stable, the stability factor has to be greater than 1, and β has to be greater than 0. The simulations show that the LNA is stable for its complete operating frequency range.

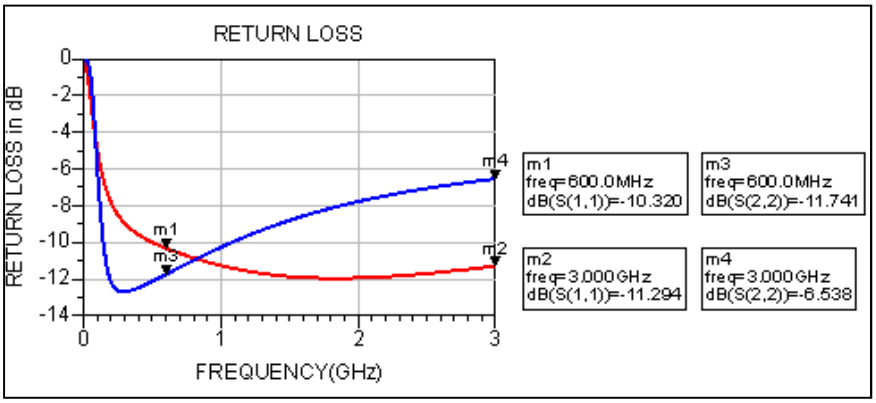


Fig. 8. Return losses S11, S22 results

Fig 8 shows return loss S11 and S22. S11 achieved is less than -10dB while S22 achieved is less than -6.5 dB. S11 and S22 are impedance matching parameters.

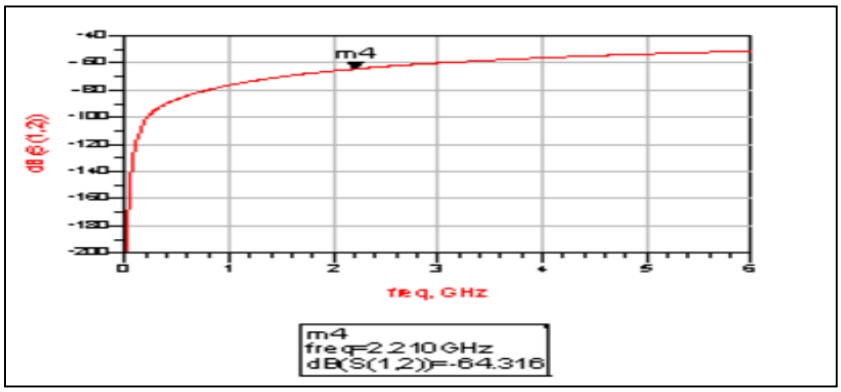


Fig. 9. Reverse isolation results

Fig 9 shows reverse isolation characteristic of LNA. An ideal LNA has infinite reverse isolation. However, reflected signals can pass through the amplifier in the reverse direction. Therefore, reverse isolation is important to quantify. The reverse isolation achieved is -64dB.

6 CONCLUSION

A wideband receiver RF CMOS LNA with feed-forward noise and distortion cancellation has been presented in this paper. Experimental results show that this technique improves the NF, gain and power dissipation of LNA, especially for LNA design in scaling down CMOS technology. The results achieved are simulated results, obtained on Agilent's ADS 2009. The core layout was designed using Micro-Wind and back-end has been completed. This work can be extended for designing Low Noise Amplifier (LNA) in different topology and the performance may be compared. Also layout of the proposed design can be fabricated and various test can be perform to verify the simulated results.

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