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# Analysis of shift register using GDI AND gate and SSASPL using Multi Threshold CMOS technique in 22nm technology

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**ABSTRACT:** Shift register in this paper possess low efficient SSASPL (Static differential Sense Amp Shared Pulsed Latch). Timing problem between pulsed latches is solved using multiple non-overlap delayed strobe signal. Here latches are grouped into several sub-shift registers. To provide better results, leakage current and leakage power are reduced with MTCMOS (Multi Threshold Complementary Metal Oxide Semiconductor) and power-delay products are further reduced using Mod-GDI(Modified Gate Diffusion Input) technique. A 16-bit shift register in 22nm technology with supply voltage VDD =200mv and consumes 0.147mW. Power consumption in percentage is 43.04% in other words power reduced in comparison to the existing systems is 14.85%. Simulation is done using Tanner EDA TOOL in 22nm technology.

**KEYWORDS:** power-delay products, SSASPL, MTCMOS, strobe signal, Mod-GDI.

## 1 INTRODUCTION

With the advent of growing technology in the communication environment achieving long battery life is of major concern in low power micro electronics such as in laptops, cellular networks and other portable systems .Major applications of shift register include image processing IC's, digital filters and communication receivers[1]. The challenging scenario lies in the nanometer technology where the reduction in supply and threshold voltage puts forth

a great demand in new design methodology in order to meet the power constraints . overweening power dissipation also leads to over heating, performance degradation and reduction of chip life and its functionality .Increased levels of integration and improvisation in feasibility and reliability with efficient cost is obtained through minimal Consumption .Static power dissipation due to reverse biased diode leakage between diffusion regions , wells and the substrate is reduced to a greater extent in this paper. In recent trends replacing flip flops with pulsed latches is practiced due to its lesser dimensions. N–bit shift register consists of N data flip flops connected in series. In this paper timing problem between pulsed latches is solved using multiple non-overlap delayed strobe signal. Latches are grouped into several sub-shift registers with a small number of pulsed clock signal and an additional temporary storage latch[1]. Modified GDI is an excellent power efficient design technique with less number of transistor counts which reduces the average power consumption and considerably decreases the delay[3].Usage of MTCMOS for designing high speed power efficient SSASPL latch is computed in 22nm technology. MTCMOS being a circuit level technique use both low threshold and high threshold voltages[2].

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## 2 ARCHITECTURE

### 2.1 PROPOSED SYSTEM

Pulsed latches used in shift register causes timing problem where all the latches are meant to have constant input signal during a clock pulse .This is overcome by using delay circuits in between the latches .Moreover delay circuits inserted between the latches increases the operating time.

One common solution is to use multiple non overlap delayed pulse clock signal therefore each latch is updated with the output of its previous one. In other words each latch uses delayed pulse clock signal compared to its previous one gradually. This in turn increases the number of delay circuits needed.

In existing system the delay between latches are generated by using a pulse clock generator which is capable of producing a number of delayed pulse clock signals which is non overlapping with one another. This concept yields a better result compared to any conventional shift registers. Also here the latches are grouped as several 4-bit sub shift register according to the need as of either 8-bit shift register or 12-bit shift registers are needed and so on. 16-bit shift register with 4 4-bit sub shift registers along with its pulse generator circuit is shown in figure 1.

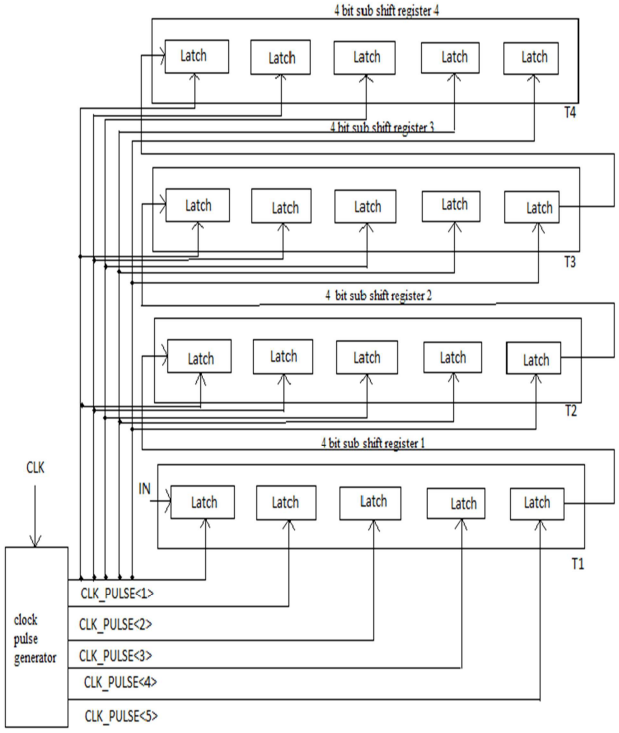


***Figure 1. 16 bit shift register***

A multiple non overlapped pulse clock signal is shown in figure 2 .(a).

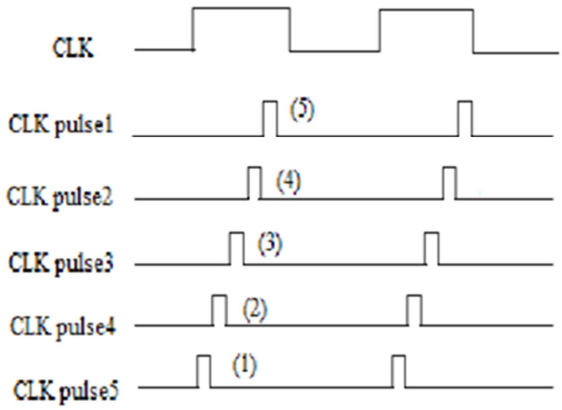


*figure 2(a):multiple non –overlapped pulse signal*

In proposed model, the width of the clock pulse is further reduced by using strobe signal instead of normal pulsed signal. Strobe signal contributes a larger reduction in power consumption required for the clock pulse to be enabled in order to activate the latch circuit. Major amount of power is consumed by latches and clock pulse circuits where each latch intakes power for data transition and for clock loading. In clocked systems, the strobe signal is treated as an enable signal for the corresponding latch or register . The data is captured on any clock edge for which the strobe or enable is active. This means that the timing is strictly relative to the clock edge. Multiple non-overlap strobe signal is shown in figure2. (b).

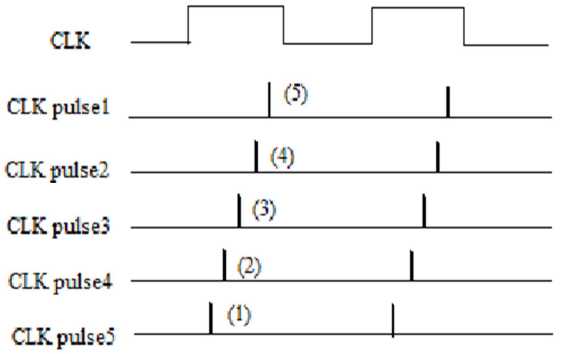


*figure 2.(b):Multiple non overlap Strobe signal*

### 2.2 DESIGN OF MTCMOS

Design of any logic circuits using MTCMOS can leads to overall enhancement in system performance [2].Digital circuits employs digital logic which is a function of present input whereas sequential logic output depends upon the present input as well as the past output which, this tells that sequential logic has memory and combinational logic does not have any memory.

Scaling of CMOS in any nanometer technology tends to reduce the required supply voltage and threshold effectively. Lowering the threshold voltage increases the sub threshold leakage current exponentially. Also reduction in number of transistors seriously retards the total power consumption of any integrated circuit due to its leakage current.

MTCMOS technology proposed here satisfies the requirement of lowering the threshold voltage and stand by current, the crucial factors necessary to obtain low power and high speed performance. MTCMOS technology employs two main features 1.PMOS and NMOS transistors are operated with two different threshold voltages within a single chip 2.two modes of operation i.e. active and sleep mode for efficient power management..General MTCMOS architecture is shown in figure 3.

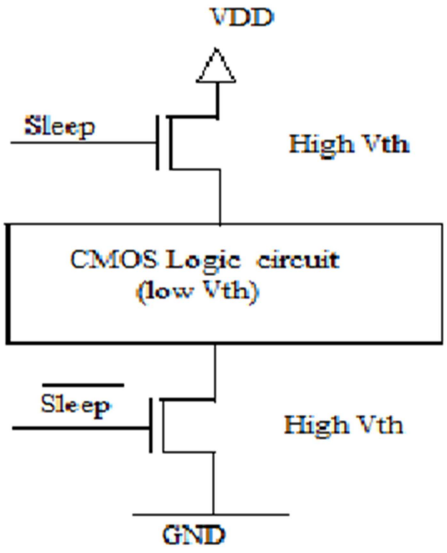


*figure 3:MTCMOS architecture*

High Vth devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. Typical high Vth devices reduce static leakage by 10 times compared with low Vth devices. Therefore only high threshold sleep transistor is used at the top and bottom of the logic circuit. Isolating the logic networks MTCMOS technique reduces the sleep mode logic power dramatically .

### 2.3 DESIGN OF GDI

New technology for low power design is Mod-GDI (Modified Gate Diffusion Input). This technique further reduces the propagation delay while maintaining low complexity of logic design . GDI based design is obtained from any conventional CMOS in such a way that the source of the PMOS and the source of the NMOS in a GDI cell is not connected to VDD and GROUND respectively.

GDI and modified GDI consists of three inputs G,P,N where G is the common gate input of PMOS and NMOS, P is the input to source or drain of PMOS and N is the input to source or drain of NMOS.GDI consumes less number of transistors compared to conventional CMOS. Basic GDI cell is shown in figure 4(a).

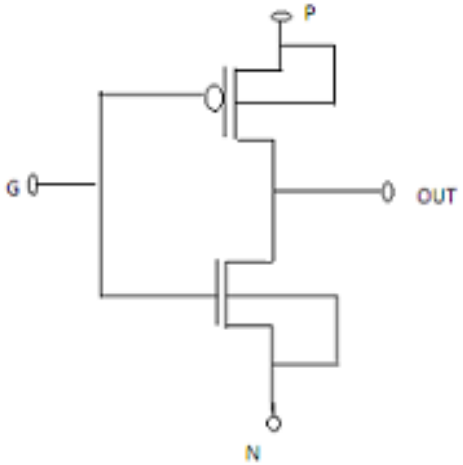


*Figure.4(a): Basic GDI cell*

Table 1 shows different logic function of the basic GDI cell based upon different input values. Thus implementation of various logic function can be realized using modified GDI with low power and high speed compared to conventional CMOS design.

***Table 1: Logic functions of GDI***

| N | P | G | OUT | FUNCTION |
|---|---|---|---|---|
| 0 | B | A | A'B | F1 |
| B | 1 | A | A'+B | F2 |
| 1 | B | A | A+B | OR |
| B | 0 | A | AB | AND |
| C | B | A | A'B+AC | MUX |
| 0 | 1 | A | A' | NOT |

GDI introduced in pulse generator of shift register is shown in figure 4(b).

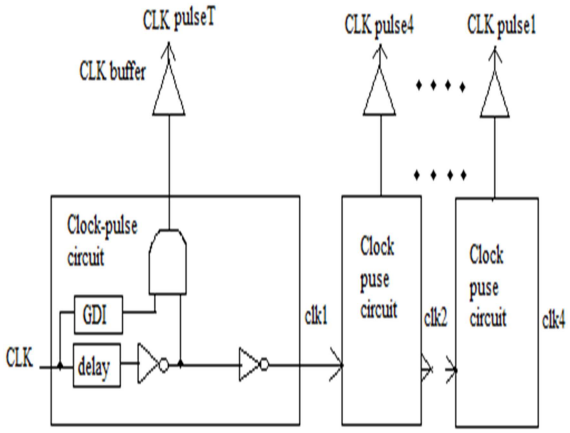


***Figure 4(b):GDI based pulse generator***

### 2.4 DESIGN OF SSASPL WITH MTCMOS

Due to parasitic capacitance and resistance short clock pulses cannot run through long shift registers. In contrast delay due to the wire increase rising and falling edge times of the clock degrading the shape of the clock pulse. A simple solution for this is to increase the clock pulse width but this decreases the maximum clock frequency .Another solution is to insert clock buffers with small wire delays but this increases area and power overhead. Moreover multiple clock pulses for multiple clock buffers increases the power overhead. Table 2 shows the general features of SSASPL latch.

***Table 2: general features of SSASPL latch***

| | |
|---|---|
| Type of pulsed latch | SSASPL |
| Word length of shift register | 256 |
| Word length of sub shift register | 4 |
| Total number of pulsed latches | 320 |
| Area | 6600 |
| Power | 1.2Mw |
| Max clock frequency | 840MHZ<br>100MHZ |

SSASPL latch using smallest number of transistors (7 transistors) consumes lowest clock pulse because it has a single transistor driven by pulsed clock signal. SSASPL updates the input data with 3 NMOS transistors and it makes use of other four transistors in cross coupled inverter manner to hold the data.

The size of PMOS and NMOS transistors in two inverters are 0.1µm and 0.5µm.SSASPL latch designed with MTCMOS is shown in figure 5.

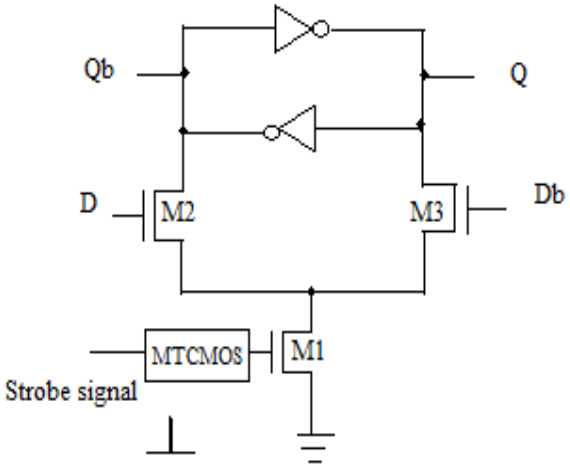


***Figure 5: Design of SSASPL latch with MTCMOS***

Conventional SSASPL latch consumes 0.10486mW power whereas SSASPL with MTCMOS technique consumes reduced power of 0.059253mW power. Thus SSASPL with MTCMOS consumes only 56.50% of power when compared to conventional SSASPL.

The overall power reduced in SSASPL when incorporating MTCMOS technique is 43.50%.

## 3 SIMULATION AND RESULTS

Here a detailed analysis of average power consumed in 16 bit shift register with MTCMOS and Modified GDI technique is proposed. Comparisons have been made between conventional master slave flip flop used shift register ,existing SSASPL based shift register and proposed 16 bit shift register based on SSASPL technique with MTCMOS technique and pulsed generator with Modified GDI have been done and successfully shown in table 3.

***Table 3 :performance comparison***

| System | Power consumed | In % |
|---|---|---|
| Conventional master slave flip flop | 0.3420mW (100%) | - |
| SSASPL based shift register | 0.1983mW | 57.89% |
| Proposed 16-bit shift register | 0.1472mW | 43.04% |

Conventional master slave flip flop used shift register schematic in tanner is shown in figure 6(a).

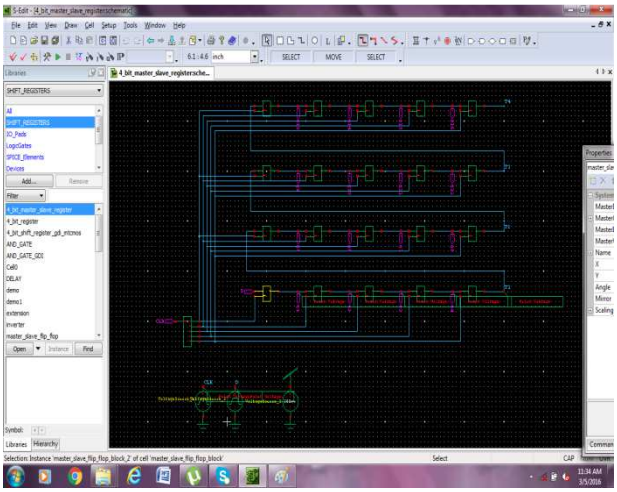

*Figure 6(a): Conventional master slave flip flop used shift register*

Output in tanner EDA tool is shown in figure 6(b)

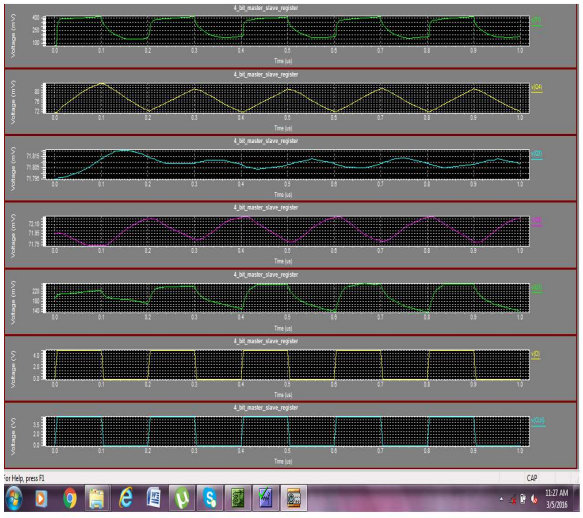

*figure 6(b) Output in Conventional master slave flip flop used shift register*

Existing SSASPL based shift register schematic is shown in tanner tool figure 7.

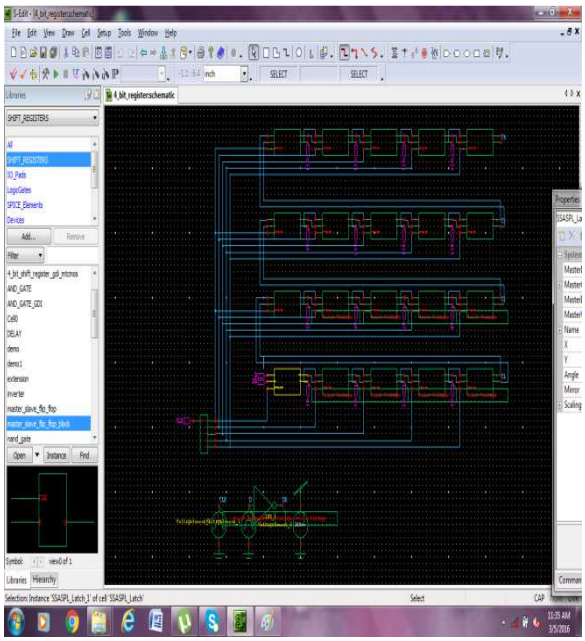

*Figure 7: Existing SSASPL based shift register*

Output for existing SSASPL technique is shown in figure 7(a).

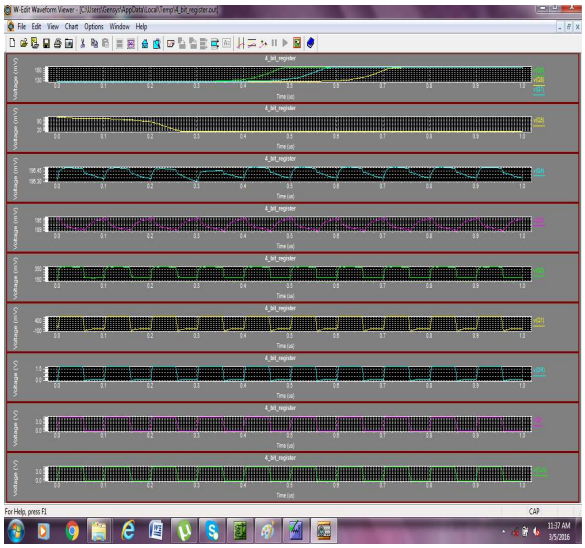

*Figure 7(a) :output for existing SSASPL technique*

Proposed 16 bit shift register based on SSASPL technique with MTCMOS technique and Modified GDI schematic is shown in figure 8.

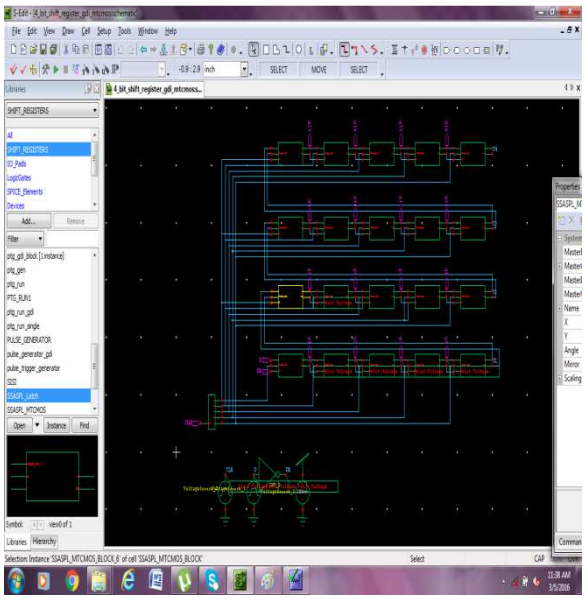

*Figure.8: proposed 16 bit shift register based on SSASPL technique with MTCMOS technique and Modified GDI.*

Output for proposed 16 bit shift register based on SSASPL technique with MTCMOS technique and Modified GDI is shown in Figure 8(b).

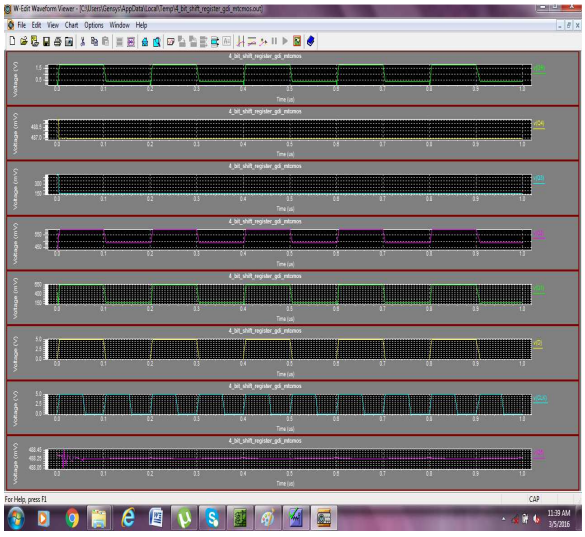

*Figure.8 output for 16-bit proposed shift register*

## 4 CONCLUSIONS

The reduction of static power consumption is achieved by replacing flip flops with pulsed latches. The timing problem between pulsed latches is reduced by using strobe signal instead of single pulsed clock signal. A 16-bit shift register in 22nm technology with supply voltage VDD =200mv and consumes 0.147mW. power consumption in percentage is 43.04% in other words power reduced in comparison to the existing systems is 14.85% . We hope the proposed method would help researchers for further research activities on shift registers.

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