International Journal of Innovation and Scientific Research
ISSN 2351-8014 Vol. 30 No. 3 May 2017, pp. 343-348

http://www.ijisr.issr-journals.org/

PERFORMANCE ANALYSIS OF VARIOUS MULTIPLIER USING VHDL

V.P. Krishnammal[1], S. Anbuselvi[2], and K. Janani[2]

[1]ASST PROF/EIE /ACE, India

[2]UG STUDENT/ EIE/ACE, India

ABSTRACT: In early days of Computers, Multiplication was implemented generally with a sequence of addition, subtraction and shift operations. Multiplier modules are common to many DSP applications. Since multipliers are rather complex circuits and must typically operate at a high system clock rate, reducing the delay of a multiplier is an essential part of satisfying the overall design. The various multiplier used are Array, Wallace and Vedic Multiplier. The Razor flip-flop is a timing fault detection technique that employs double sampling by the main and shadow Flip-Flops. Different types of multiplier are going to implement using XILINX ISE Design Suite 14.5 software and the performance will analysed with ordinary multiplier.

KEYWORDS: Ripple Carry (RCA) Adder, Vedic Multiplier (VM), Urdhava Tiryakbhyam Sutra, Array Multiplication.

1 INTRODUCTION

The vast variety of application areas for multipliers exbits different requirements for Speed, Area, Power consumption and other specifications. Based on these requirements which are imposed from the system that the multiplier will be operating in, different characteristic of the multiplier will be given different priorities.

Multipliers are key components of many high performance systems such as microprocessors, digital signal processors and FIR filter system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system This is even more important for Battery-powered applications where the energy budget is extremely limited. Low-power design has become a new area in VLSI technology and power-aware design is inevitable in the new Electronic Design Automation(EDA) tools.

2 MULTIPLIER

In this paper a simple 8 bit digital multiplier is proposed which is based on Urdhva Tiryakbhyam (Vertically Crosswise) Sutra, of the Vedic Maths. Two binary numbers (8-bit each) are multiplied with this Sutra. The simplest scheme for multiplication, known as shift-and-add scheme, consists of cycles of shifting and adding with hardware or software control loops. Razor relies on a combination of architecture and circuit level techniques for efficient error detection and correction of delay path failures. The main flip-flop and shadow latch will latch the correct data

Array multiplier is taken which is to compare the results with Vedic multipliers. The results are compared in terms of power, delay and area. The timing report of the performed multiplier has been given as an input for the razor flip-flop.

2.1 ARRAY MULTIPLIER

Array multiplier is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added.

Corresponding Author: V.P. Krishnammal

The addition can be performed with normal carry propagate adder. N-1 adders are required where N is the multiplier length.

				A3	A2	A1	A0	Inputs
			x	B3	B2	B1	B0	
			C	B0 x A3	B0 x A2	B0 x A1	B0 x A0	Internal Signals
		+	B1 x A3	B1 x A2	B1 x A1	B1 x A0		
		C	sum	sum	sum	sum		
	+	B2 x A3	B2 x A2	B2 x A1	B2 x A0			
	C	sum	sum	sum	sum			
+	B3 x A3	B3 x A2	B3 x A1	B3 x A0				
C	sum	sum	sum	sum				
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Outputs

Fig. 1.

Although the method is simple as it can be seen from this example, the addition is done serially as well as in parallel. To improve on the delay and area the CRAs are replaced with Carry Save Adders, in which every carry and sum signal is passed to the adders of the next stage. Final product is obtained in a final adder by any fast adder (usually carry ripple adder). In array multiplication we need to add, as many partial products as there are multiplier bits.

2.2 WALLACE TREE MULTIPLIER

Several popular and well-known schemes, with the objective of improving the speed of the parallel multiplier, have been developed in past. Wallace introduced a very important iterative realization of parallel multiplier. This advantage becomes more pronounced for multipliers of bigger than 16 bits.

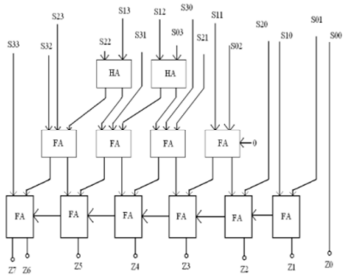


Fig. 2. bit Wallace architecture

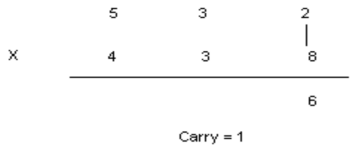
2.3 VEDIC MULTIPLIER

Vedic mathematics is also known as “speed mathematics”. This type of mathematics is used to reduce the time consumption. The word ‘Vedic‘ is derived from the word ‘Veda’ which means store-house of all knowledge. Ancient and medieval Indian mathematical works, all composed in Sanskrit, usually consist of a section of Sutras in which a set of rules or problems were stated with great economy in verse in order to aid memorization by a student.

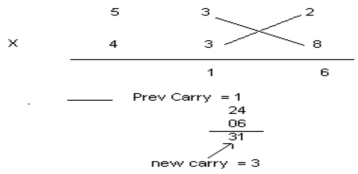
The design starts first with Multiplier design, that is 2x2 bit Multiplier. Here “urdhva Tiryakbhyam Sutra” or “Vertically and crosswise Algorithm” for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is quite different from the traditional method of multiplication, that is to add and shift the partial products. This sutras shows how to handle the multiplication of larger number by breaking into the smaller number of size. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed.

EXAMPLE FOR URDHVA TIRYAKBHYAM SUTRA

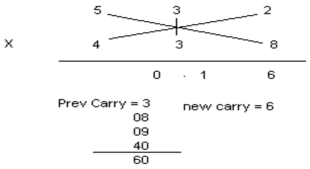
Step 1



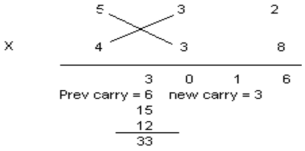
Step 2



Step 3



Step 4



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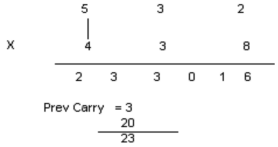

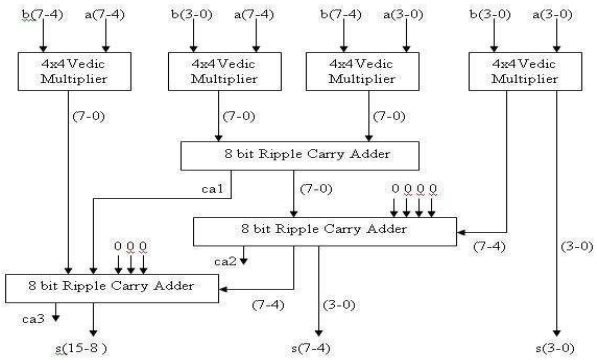

Fig. 3. Vedic Multiplier for 8x8 bit Module using carry save adder

3 RAZOR FLIP FLOP

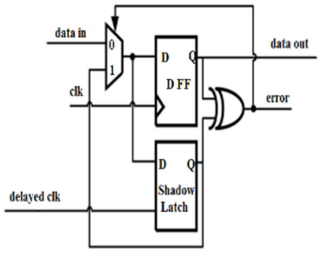

Fig. 4. Diagram for Razor Flip Flop

A combination of circuit and architectural techniques for low cost in-situ error detection and correction of delay failures. At the circuit level, each delay-critical flip-flop is augmented with a so-called shadow latch which is controlled using a delayed clock. The operating voltage is constrained such that the worst-case delay is guaranteed to meet the shadow latch setup time, even though the main flip-flop could fail. The razor technology is a breakthrough work, which largely eliminates the safety margins by achieving variable tolerance through in situ timing error detection and correction ability .This approach is based on a razor flip-flop, which detects and corrects delay errors by double sampling.

4 SIMULATION AND RESULT

4.1 SIMULATION FOR ARRAY MULTIPLIER

The output response of array multiplier is shown in figure 4.1

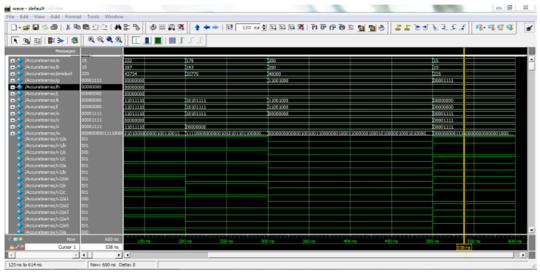

Fig. 5. output for 8 bit array multiplier

4.2 SIMULATION FOR VEDIC MULTIPLIER

The output response of vedic multiplier is shown in figure 4.2

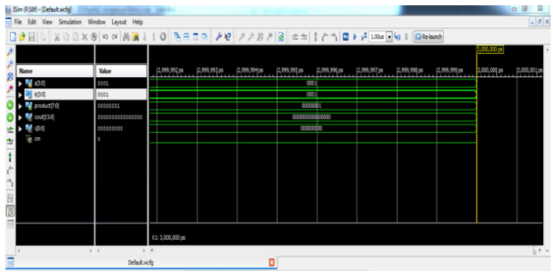

Fig. 6. output for 8 bit vedic multiplier

4.3 SIMULATION FOR ARRAY MULTIPLIER WITH RAZOR

The output response of array multiplier with razor is shown in figure 4.3

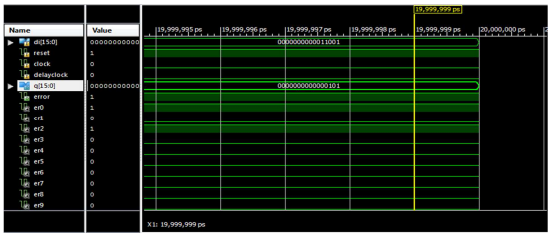

Fig. 7. output for 8 bit array multiplier with razor

4.4 SIMULATION FOR VEDIC MULTIPLIER WITH RAZOR

The output response of Vedic multiplier with razor is shown in figure 4.4

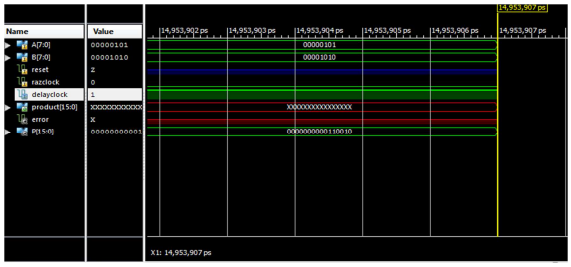

Fig. 8. output for 8 bit vedic multiplier with razor

4.5 RTL DIAGRAM FOR VEDIC MULTIPLIER

The schematic diagram of RTL for Vedic Multiplier is showm in fig4.5

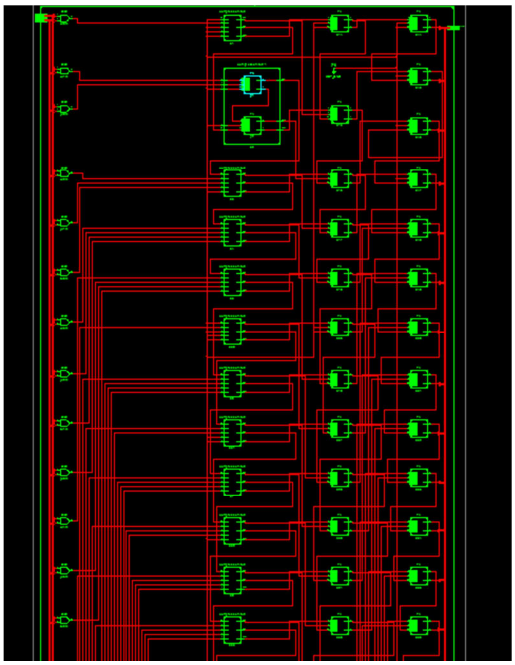

Fig. 9. RTL Diagram for Vedic multiplier

5 RESULT AND DISCUSSION

	Array Multiplier	Wallace Multiplier	Vedic Multiplier
Memory Usage	236Mb	216Mb	146Mb
Time Delay	21.689ns	20.34ns	16.70ns
Power Report	16.57mw	15.88mw	14.23mw

6 CONCLUSION

This sutra is applicable to all cases of multiplication. The results show that Urdhava Tiryakbhyam sutra used to implement high speed complex multiplier efficiently in digital signal processing algorithms by decreasing propagation delay (ns). The Vedic multiplier is much more efficient than Array multiplier in terms of execution time (speed). An awareness of Vedic mathematics can be effectively increased if it is included in engineering education. In future, all the major universities may setup appropriate research centers to promote research works in Vedic mathematics.

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