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Modeling And Analysis Of Series-Switch Five-Level Dual-Buck Full-Bridge Inverters For Grid-Tied Applications

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ABSTRACT: Dual-buck inverters feature some attractive merits, such as no reverse recovery issues of the body diodes and free of shoot-through. However, since the filter inductors of dual-buck inverters operate at each half cycle of the utility grid alternately, the inductor capacity of dual-buck inverters is twice as much as H-bridge inverters. Thus, the power density of dual-buck converters needs to be improved, as well as the conversion efficiency.

The detailed derivation process of two five-level full-bridge topology modeling is presented. The operation modes, modulation methods and control strategies of the series-switch five-level DBFBI topology are analyzed in detail. The THIPWM technique operates by adding a third harmonic component to the sinusoidal modulating wave. It is possible to increase the fundamental by about 15.5% and hence, allow a better utilization of the DC power supply.

The power device losses of the three-level DBFBI topology and five-level DBFBI topologies, with different switching frequencies are calculated and compared. Both the relationship between the neutral point potential self-balancing and the modulation index of inverters are revealed. Simulation results have shown that the five-level series DBFBI topology exhibit higher efficiency than the five-level H-bridge inverter topology and the three-level DBFBI topology.

KEYWORDS: Series-switch five-level DBFBI topology modeling, Switching State Analysis, Power losses and efficiency, THIsine PWM and THI reduction

1 INTRODUCTION

The multilevel technique is an effective way to achieve high power density. There are three widely used topologies of single-phase multilevel inverters, diode neutral point clamped (DNPC) multilevel inverters, flying capacitor clamped (FCC) multilevel inverters and active neutral point clamped (ANPC) multilevel inverters. The basic concept of the above three multilevel topologies is to use smaller rating power devices to generate appreciable high-level output voltage waveforms. However, conventional multilevel inverters require a large number of power devices and auxiliary dc links when the output voltage levels are higher than three-level.

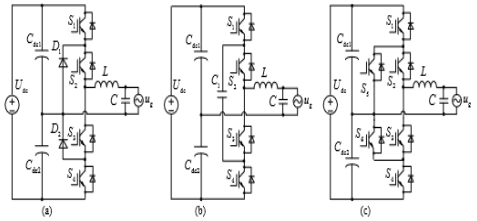


Fig.1Three popular topologies of H-bridge multilevel inverters.
(a) Diode neutral point clamped (DNPC) (b) Flying capacitor clamped (FCC) (c) Active neutral point clamped (ANPC)

A five-level H-bridge inverter topology was proposed by introducing a neutral point clamped bi-directional switch (NPC branch) based on the existing conventional full-bridge inverter. Comparing with the DNPC five-level inverter topology, the FCC five-level inverter topology, and the ANPC five-level inverter topology, the number of power devices in the new five-level H-bridge inverter has been reduced significantly.

The series-switch five-level DBFBI topology is taken for analysis in terms of the operation principle and the THIsine PWM modulation method. Simulation results were obtained to evaluate the performance and harmonic reduction.

2 FIVE-LEVEL SERIES DBFBI-TOPOLOGY MODELLING

The conventional three-level full-bridge inverter is combined with a two-level capacitive voltage divider and NPC branch. The nodes of the capacitive voltage divider, P1, N1 and O1, are connected to the nodes, P2, N2 and O2, respectively. The node of the NPC branch A1 is connected to the node of the three-level DBFBI A2.

By employing the topology generation above rule, a three-level DBFBI topology is combined with a two-level capacitive voltage divider and a NPC branch, as shown in Fig.2

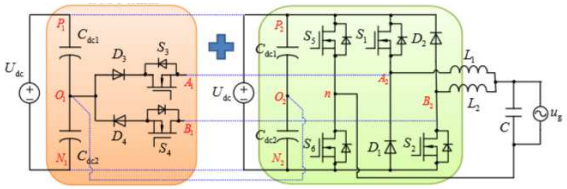


Fig.2. The topology generation: three-level DBFBI combined with a two-level capacitive voltage divider and a NPC branch

The node of the NPC branch B1 is connected to the node of the three-level DBFBI B2. Then, the redundant capacitors, Cdc1 and Cdc2, can be removed. As a result, a NPC five-level DBFBI topology is generated.

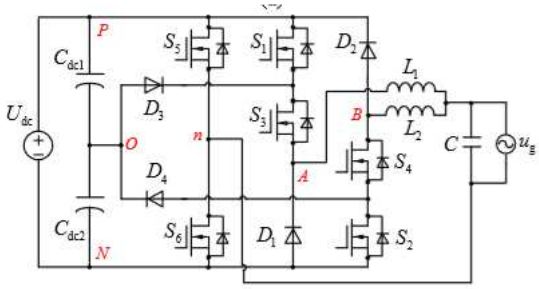


Fig.3. Series-switch five-level DBFBI topology

Compared with the three-level DBFBI topology there are two additional switches and two additional diodes in the proposed NPC five-level DBFBI topology.

3 ANALYSIS ON THE SERIES-SWITCH FIVE-LEVEL DBFBI TOPOLOGY

SWITCHING STATE ANALYSIS

The Series-switch five-level DBFBI topology is taken as an example for detailed analysis. The key waveforms of the Series-switch five-level DBFBI are shown in Fig.4. Two reference signals, ur1 and ur2, are compared with a carrier signal to produce THIsine pulse width modulation (PWM) signals for the switches. ugS1 to ugS6 represent the gate drive signals of power switches S1 to S6.

In order to avoid the shoot-through problem, the dead time has been set within the drive signals of the switches S5 and S6. uAn represents the voltage difference between the node A and node n, and uBn is the voltage difference between the node B and node n. Two filter inductors, L1 and L2, are operating at each half cycle of the utility grid alternately. Therefore, uAB-n is defined as the output levels of the DBFBI topologies, and uAB-n is represented as,

$$u_{AB-n} = u_{An} + u_{Bn} - u_g \quad (1)$$

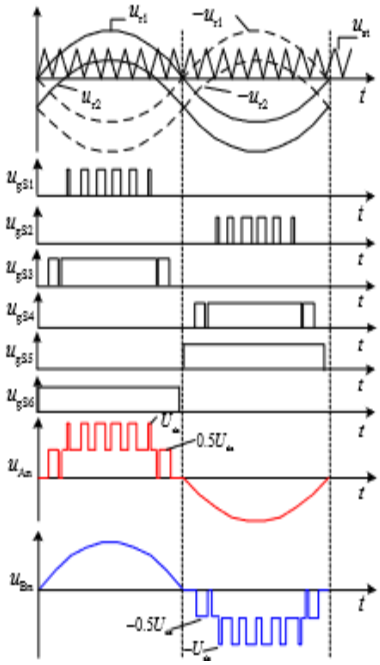


Fig.4.Key waveforms of the series-switch five-level DBFBI topology.

On the other hand, the series-switch five-level DBFBI topology is operating with unity power factor. In order to avoid the inductor current distortion, at the beginning of the positive half cycle of the utility grid, the switches S1, S3 and S6 are turned ON at the same time. At the end of the positive half cycle, the switch S3 is turned OFF before the switch S6, and the current of inductor L1 decreases to zero naturally. Similarly, at the beginning of the negative half cycle of the utility grid, the switches S2, S4 and S5 are turned ON at the same time. Since the series-switch five-level DBFBI topology is digitally controlled, this modulation method is easy to implement.

Furthermore, it is also suitable to both the NPC five-level DBFBI topology, the series-diode five-level DBFBI topology, and the family of five-level DBFBI topologies with high reliability. The series-switch five-level DBFBI has six operation modes, which are shown in Fig 5.

$$L_1 \frac{di_{L1}}{dt} = U_{dc} - u_g \quad (2)$$

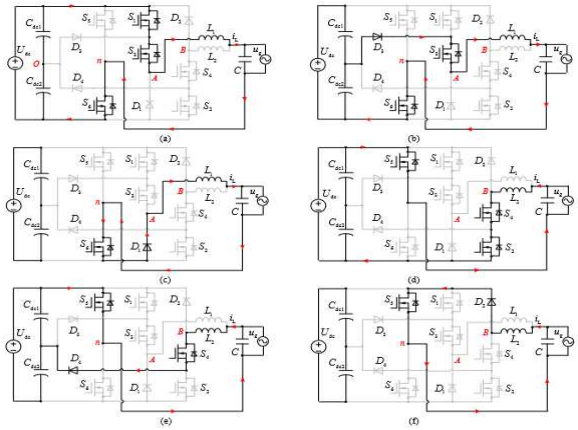


Fig.5 Equivalent circuits of switching state.
(a) State #1. (b) State #2. (c) State #3. (d) State #4. (e) State #5. (f) State #6.

(1) State #1 . Maximum positive output, uAn=Udc. There is no current flowing through the inductor L2, thus the voltage on the inductor L2 is equal to zero, and uBn=ug>0. As a result, uAB-n=Udc. S1, S3 and S6 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig.5. The reverse blocking voltage on D3 is equal to 0.5Udc, and the reverse blocking voltage on D1 is equal to Udc. The drain-source voltage on S5 is equal to Udc. During this state, the inductor current iL1 increases linearly

(2) State #2 Half-level positive output, uAn=0.5Udc. There is no current flowing through the inductor L2, thus the voltage on the inductor L2 is equal to zero, and uBn=ug>0. As a result, uAB-n=0.5Udc. S3 and S6 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.5.The drain-source voltage on S1 is equal to 0.5Udc, and the reverse blocking voltage on D1 is equal to 0.5Udc. During this state, the inductor current iL1 decreases linearly when the voltage of the utility grid is higher than 0.5Udc

$$-L_1\frac{di_{L1}}{dt}=\frac{U_{dc}}{2}-u_g \quad (3)$$

The inductor current iL1 increases linearly when the voltage of the utility grid is lower than 0.5Udc

$$L_1\frac{di_{L1}}{dt}=\frac{U_{dc}}{2}-u_g \quad (4)$$

(3) State #3 .Zero output at the positive half period of the utility grid, uAn=0. There is no current flowing through the inductor L2, thus the voltage on the inductor L2 is equal to zero, and uBn=ug>0. As a result, uAB-n=0. S6 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.5 Both the drain-source voltages on S1 and S3 are equal to 0.5Udc. During this state, the inductor current iL1 decreases linearly

$$L_1\frac{di_{L1}}{dt}=-u_g \quad (5)$$

(4) State #4 Zero output at the negative half period of the utility grid, uBn=0. There is no current flowing through the inductor L1, thus the voltage on the inductor L1 is equal to zero, and uAn=ug<0. As a result, uAB-n=0. S5 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.5 Both the drain-source voltages on S2 and S4 are equal to 0.5Udc. During this state, the inductor current iL2 increases linearly

$$L_2\frac{di_{L2}}{dt}=-u_g \quad (6)$$

(5) State #5 Half-level negative output, uBn=-0.5Udc. There is no current flowing through the inductor L1, thus the voltage on the inductor L1 is equal to zero, and uAn=ug<0. As a result, uAB-n=-0.5Udc. S4 and S5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.5 .The drain-source voltage on S2 is equal to 0.5Udc, and the reverse blocking voltage on D2 is equal to 0.5Udc. During this state, the inductor current iL2 decreases linearly when the voltage of the utility grid is lower than 0.5Udc

$$-L_2\frac{di_{L2}}{dt}=-\frac{U_{dc}}{2}-u_g \quad (7)$$

The inductor current iL2 increases linearly when the voltage of the utility grid is higher than 0.5Udc

$$L_2\frac{di_{L2}}{dt}=-\frac{U_{dc}}{2}-u_g \quad (8)$$

(6) State #6. Maximum negative output, uBn=-Udc. There is no current flowing through the inductor L1, thus the voltage on the inductor L1 is equal to zero, and uAn=ug<0. As a result, uAB-n=-Udc. S2, S4 and S5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.5. The reverse blocking voltage on D4 is equal to 0.5Udc, and the reverse blocking voltage on D2 is equal to Udc. During this state, the drain-source voltage on S6 is equal to Udc. In this mode, the inductor current iL2 decreases linearly

$$-L_2\frac{di_{L2}}{dt}=-U_{dc}-u_g \quad (9)$$

Based on the equations (2) to (9), it can be seen that the voltage jump of filter inductors is 0.5Udc, and the duty cycles of switches, S1 to S4, can be derived as,

Table 1.

	NPC	Series-switch	Series-diode	H-bridge
u_{S1}, u_{S2}	U_{dc}	$0.5U_{dc}$	U_{dc}	U_{dc}
u_{S3}, u_{S4}	$0.5U_{dc}$	$0.5U_{dc}$	$0.5U_{dc}$	U_{dc}
u_{S5}, u_{S6}	U_{dc}	U_{dc}	U_{dc}	$0.5U_{dc}(S_x)$
u_{D1}, u_{D2}	U_{dc}	U_{dc}	$0.5U_{dc}$	$0.25U_{dc}$
u_{D3}, u_{D4}	U_{dc}	$0.5U_{dc}$	U_{dc}	$0.25U_{dc}$

THE MAXIMUM VOLTAGE STRESSES OF THE POWER DEVICES IN BOTH DBFBI TOPOLOGIES AND THE H-BRIDGE TOPOLOGY

$$\begin{cases} d_{S1} = (2u_g / U_{dc}) - 1 & u_g > 0.5U_{dc} \\ d_{S2} = (-2u_g / U_{dc}) - 1 & -u_g > 0.5U_{dc} \\ d_{S3} = 2u_g / U_{dc} & 0 < u_g < 0.5U_{dc} \\ d_{S4} = -2u_g / U_{dc} & -0.5U_{dc} < u_g < 0 \end{cases} \quad (10)$$

From the above operation analysis, there is no current flowing through the body diodes of the switches. Therefore, compared with the conventional five-level H-bridge inverter topology shown in Fig.2, the presented five-level DBFBI topologies are free of reverse recovery problem in the freewheeling mode, and the MOSFETs with low on-resistances can be used instead of IGBTs.

In addition, compared with the three-level DBFBI topology, the voltage jump of each high-frequency switch in the presented five-level DBFBI topology is only half of the input voltage.

Therefore, the switching loss of the presented five-level DBFBI topology is much lower than that of the three-level DBFBI topology. Furthermore, the voltage jump of each inductor in the presented five-level DBFBI topology is only half of the input voltage as well, which means this topology

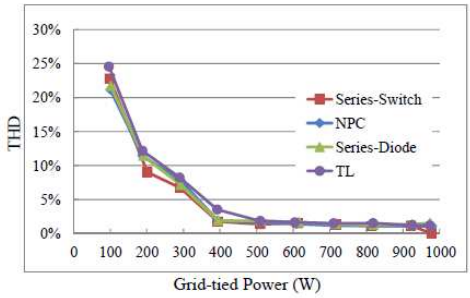


Fig.6. THD comparison of the three-level DBFBI and three proposed five-level DBFBI topologies

4 SIMULATION AND RESULTS

A series-switch five-level dual-buck full-bridge inverters model simulation obtained with number of outputs, less harmonic distortions and reduced the switches using simulink developed by Math works

The gating pulses trigger thyristors to convert input dc to ac supply. Output filters are also used. The THIPWM Technique was used .

Table 2. PARAMETERS OF THE SIMULATION PROTOTYPE

Parameter	Value
Input voltage	350~450V
Grid voltage	230V/50Hz
Grid frequency	50Hz
Rated power	1kW
Switching frequency	40kHz
Three-level filter inductor L_1&L_2	4mH
Five-level filter inductor L_1&L_2	2mH
Filter Capacitor C_o	0.47uF
High-voltage MOSFET	SPW47N60C3(650V)

In order to make a trade-off between the power density and the efficiency, the switching frequency of these three inverters were set at 40kHz. The YOKOGAWA WT1800 power analyzer was used to measure the efficiencies of these inverters.

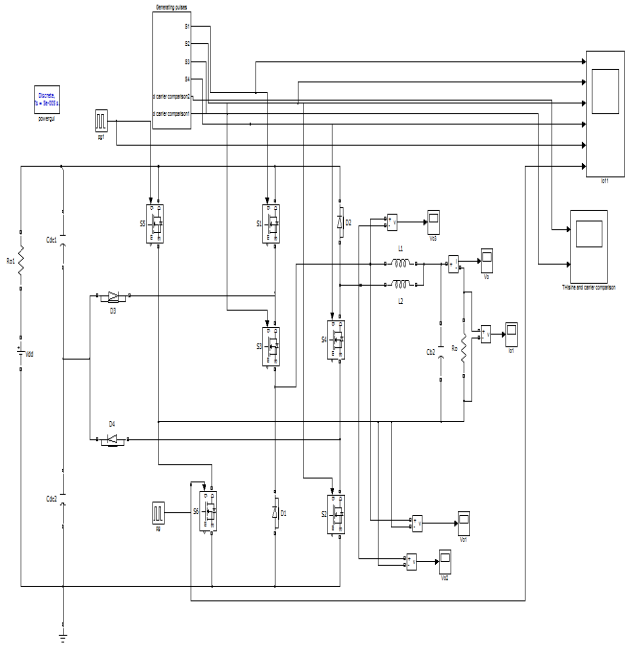


Fig 7:Simulation circuit diagram

5 RESULTS

The various wave forms voltage, current and pulses are discussed below

Gate pulses:

The gate pulses for S1 to S6 are below

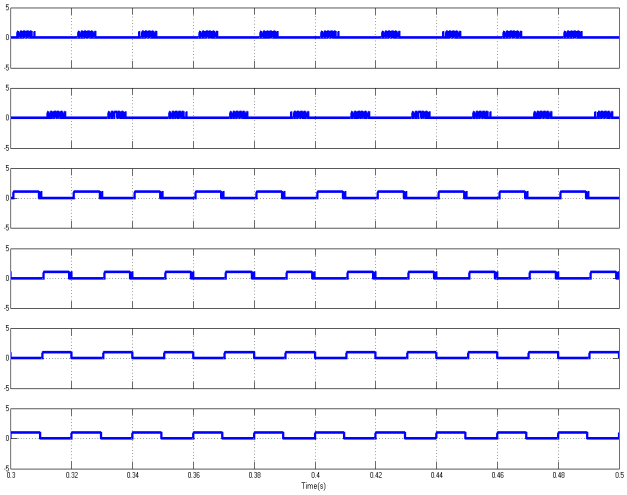


Fig 8 Gate pulses for S1 to S6

THIsine and carrier comparison:

Here the PWM technique used is THIPWM and it is generated as

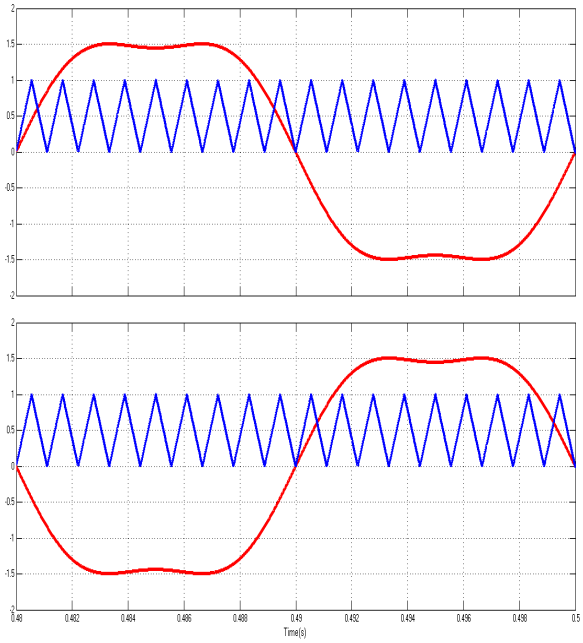
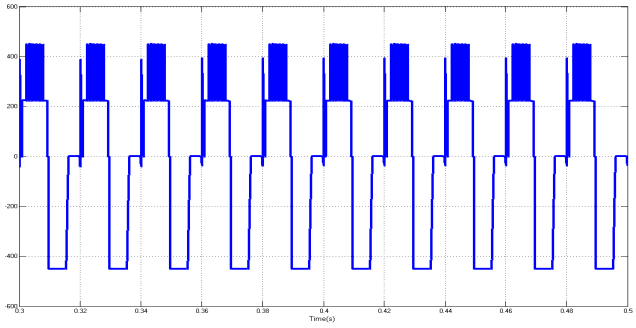


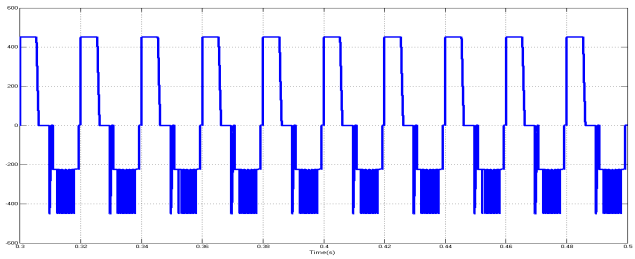
Fig 9 THIPWM

Voltage on inductors:

Vo1:



Vo2:



Vo3:

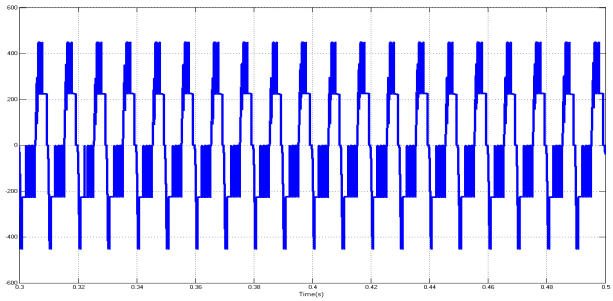
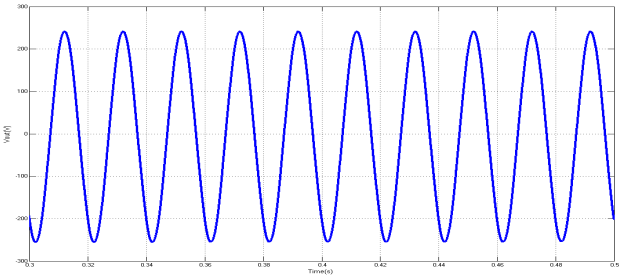


Fig 10 Voltage on inductors

Output voltage:



Output current:

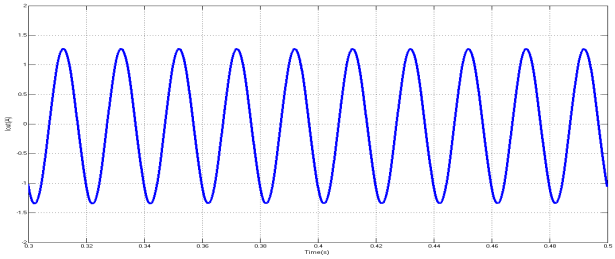


Fig 11 Output voltage and current for voltage wave form

6 CONCLUSION AND FUTURE WORK

The Series-switch five-level dual-buck full-bridge inverters has been proposed in this project. The detailed derivation processes of two five-level full-bridge topology generation rules, including conventional full-bridge inverters and dual-buck full-bridge inverters, have been presented and explained

The two-level half-bridge inverter is replaced by a two-level dual-buck half-bridge inverter, and a family of five-level DBFBI topologies with high reliability has been generated. Furthermore, the relationship between the NP potential self-balancing and the modulation index of inverters are revealed. Simulation results have verified that the five-level DBFBI topologies have the following advantages:

(1) Compared with the three-level DBFBI, the voltage jumps of high-frequency switching devices and the filter inductances are only half. Therefore, the family of five-level DBFBI topologies requires lower power rating devices and smaller filter inductors, which result in higher conversion efficiency and higher power density

(2) The series-switch five-level DBFBI has the highest efficiency compared with the three-level DBFBI, the conventional five-level H-bridge inverter, the NPC five-level DBFBI and the series-diode five-level DBFBI. Hence, the family of five-level DBFBI topologies is an attractive solution for grid-tied renewable generation systems with high efficiency and high power density

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